

Figure 4.1 The tutor2.gdf schematic.

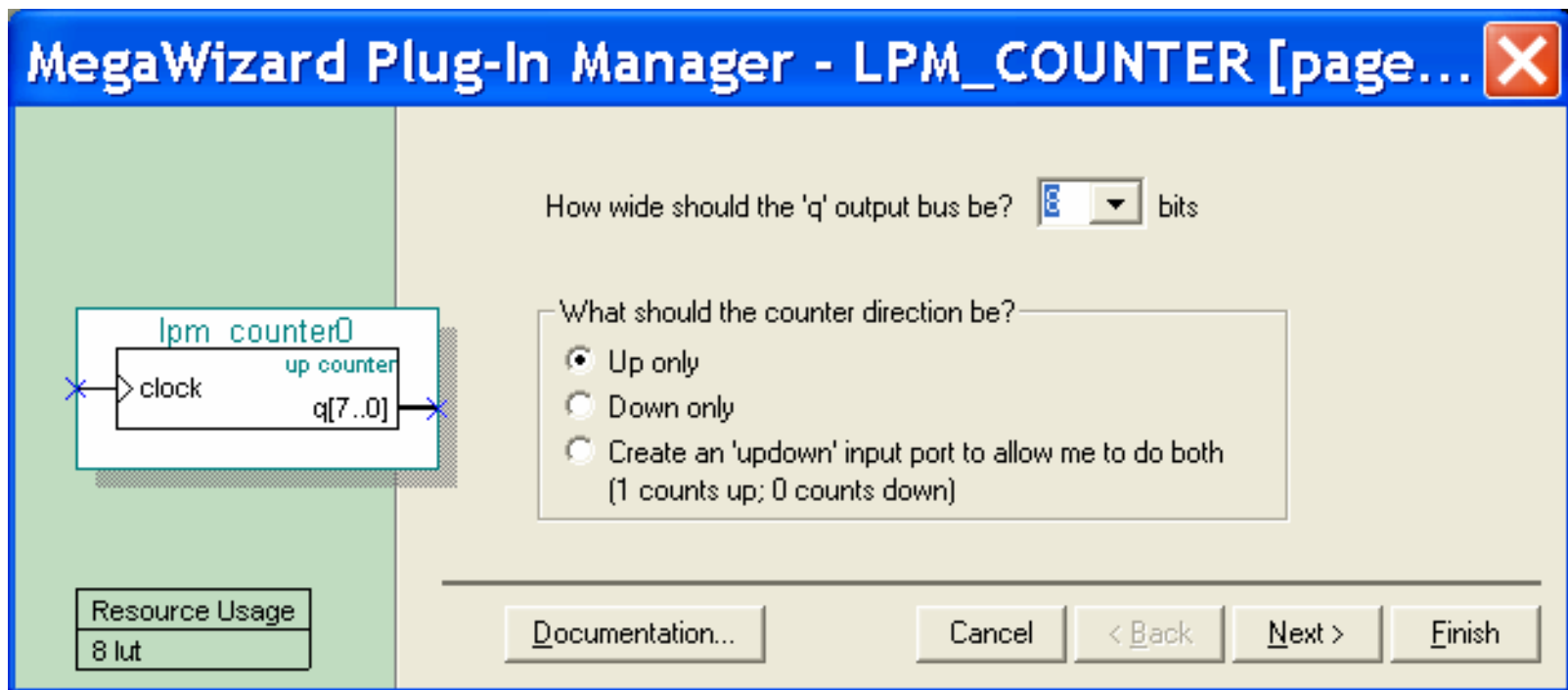


Figure 4.2 Lpm_counter0 MegaWizard edit window.

```
Quartus II - C:/qbooksoft/CHAP4/tutor3 - tutor3 - [LCD_Display.vhd]
File Edit View Project Assignments Processing Tools Window Help
tutor3
tutor3.bdf LCD_Display.vhd
102 PROCESS (CLK_400HZ, reset)
103 BEGIN
104     IF reset = '0' THEN
105         state <= RESET1;
106         DATA_BUS_VALUE <= X"38";
107         next_command <= RESET2;
108         LCD_E <= '1';
109         LCD_RS <= '0';
110         LCD_RW_INT <= '1';
111
112     ELSIF CLK_400HZ'EVENT AND CLK_400HZ = '1' THEN
113 -- State Machine to send commands and data to LCD DISPLAY
114         CASE state IS
115 -- Set Function to 8-bit transfer and 2 line display with 5x8 Font size
116 -- see Hitachi HD44780 family data sheet for LCD command and timing details
117             WHEN RESET1 =>
118                 LCD_E <= '1';
119                 LCD_RS <= '0';
120                 LCD_RW_INT <= '0';
121                 DATA_BUS_VALUE <= X"38";
122                 state <= DROP_LCD_E;
123                 next_command <= RESET2;
124                 CHAR_COUNT <= "00000";
125             WHEN RESET2 =>
126                 LCD_E <= '1';
127                 LCD_RS <= '0';
128                 LCD_RW_INT <= '0';
129                 DATA_BUS_VALUE <= X"38";
130                 state <= DROP_LCD_E;
131                 next_command <= RESET3;
132             WHEN RESET3 =>
133                 LCD_E <= '1';
```

System Processing
Message: 0 of 265
Location: Locate
For Help, press F1
Ln 1, Col 1 Idle NUM

Figure 4.3 Internal VHDL code for LCD_Display function.

| Entity | Logic Cells | LC Registers | Memory Bits | Pins | Virtual Pins | LUT-Only LCs | Register-Only LCs | LUT/Register LCs | Carry Chain LCs |
|----------------------|-------------|--------------|-------------|------|--------------|--------------|-------------------|------------------|-----------------|
| Cyclone: EP1C6Q240C8 | | | | | | | | | |
| tutor2 | 119 (0) | 67 | 0 | 14 | 0 | 52 (0) | 1 (0) | 66 (0) | 33 (0) |
| LCD_Display:inst1 | 111 (86) | 59 | 0 | 0 | 0 | 52 (52) | 1 (1) | 58 (33) | 25 (0) |
| lpm_counter0:inst2 | 8 (0) | 8 | 0 | 0 | 0 | 0 (0) | 0 (0) | 8 (0) | 8 (0) |

Figure 4.4 Hierarchy display of the tutor2 design.

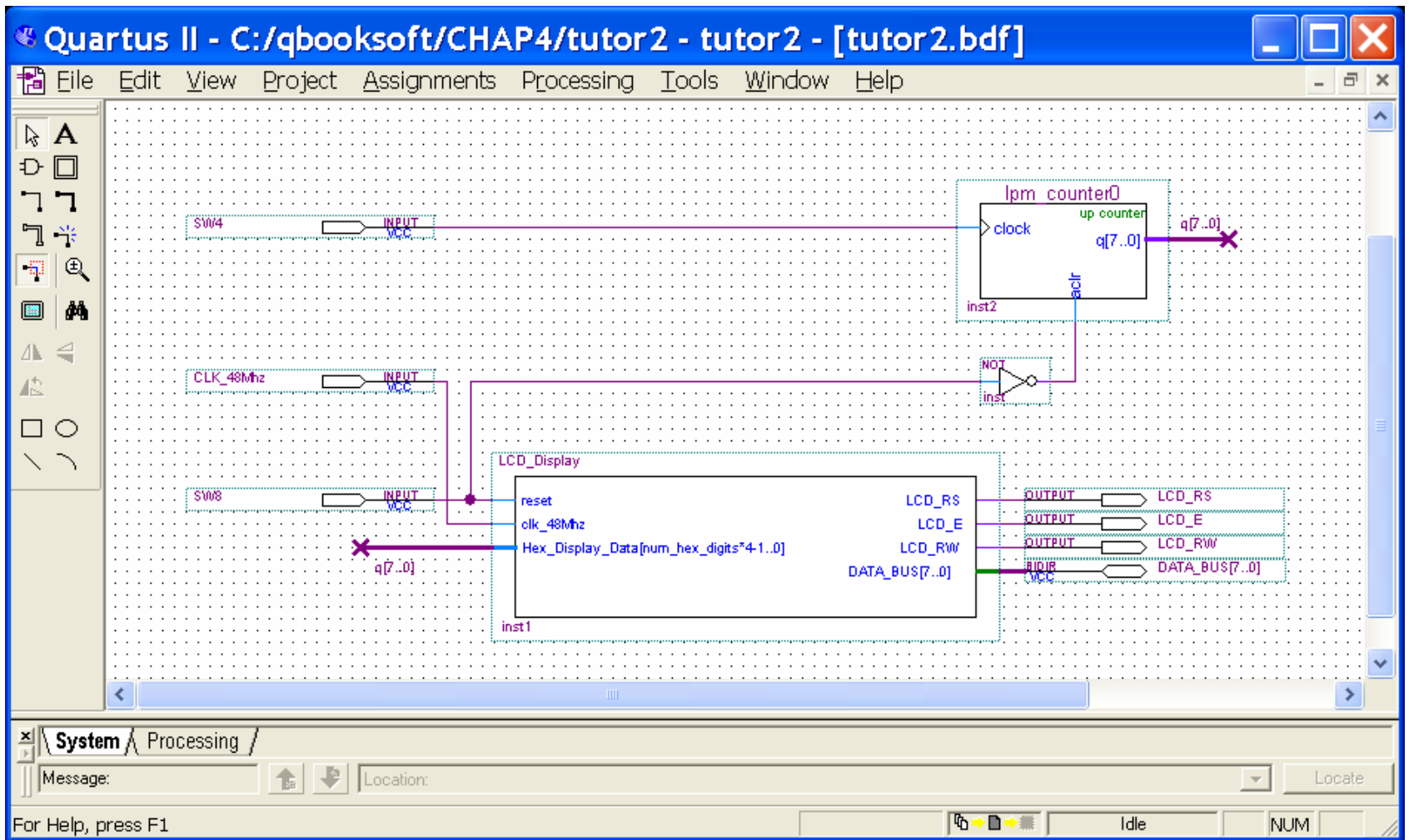


Figure 4.5 Enlarged view of tutor2 design showing bus connections.

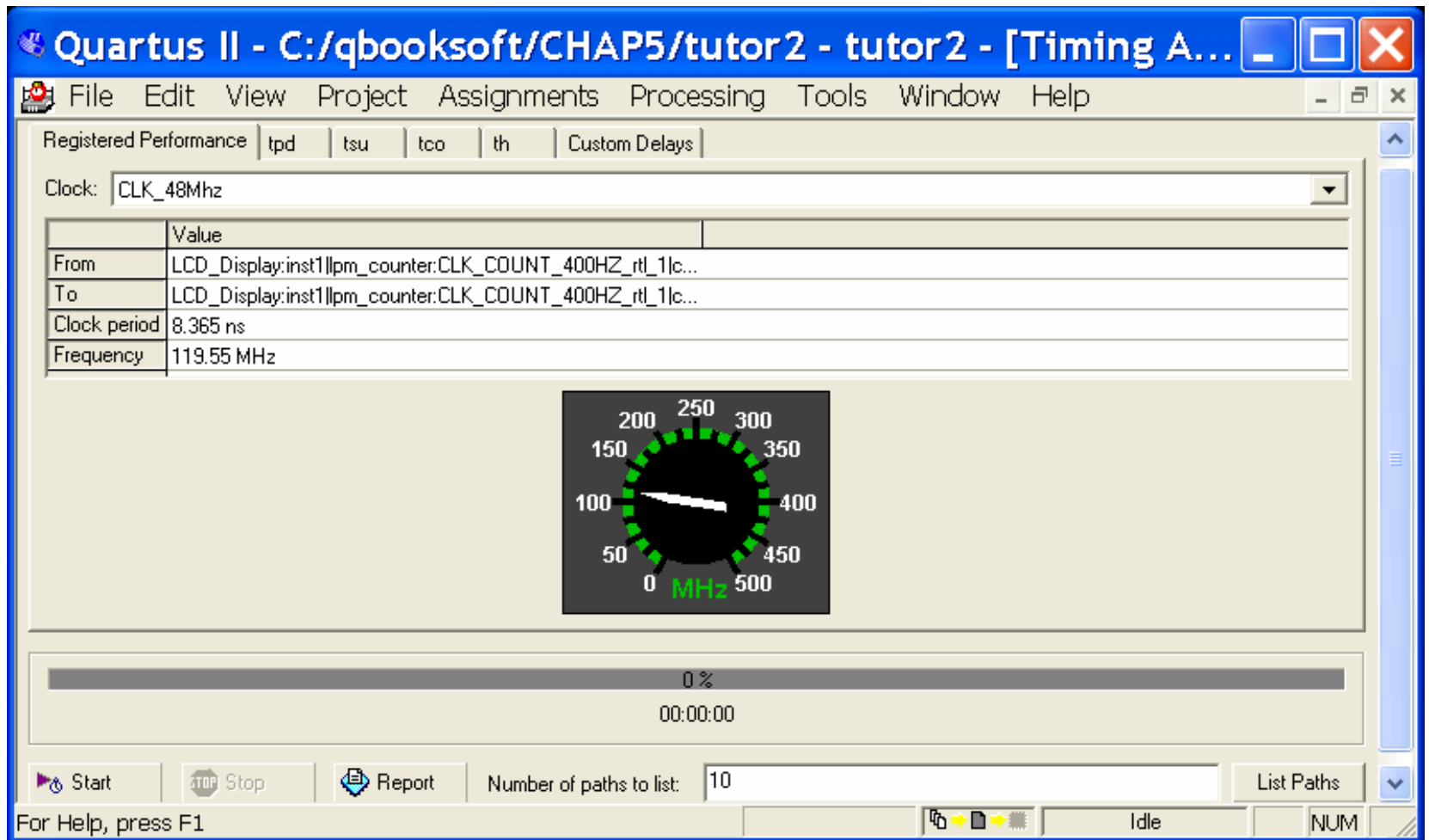


Figure 4.6 Timing analysis of a Sequential Circuit.

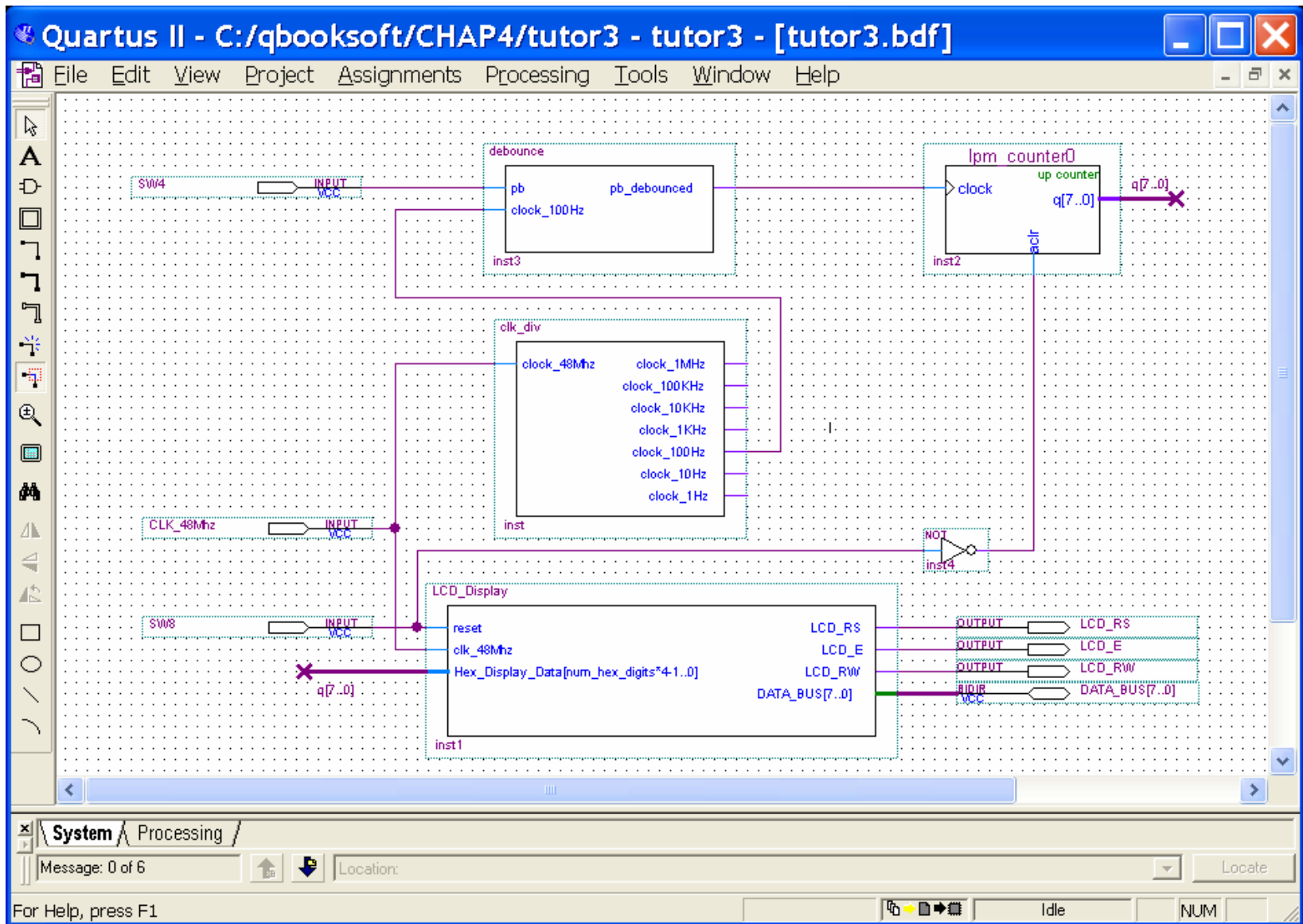


Figure 4.8 Modified tutor2 design schematic.