

Figure 3.1 Digital logic technologies.

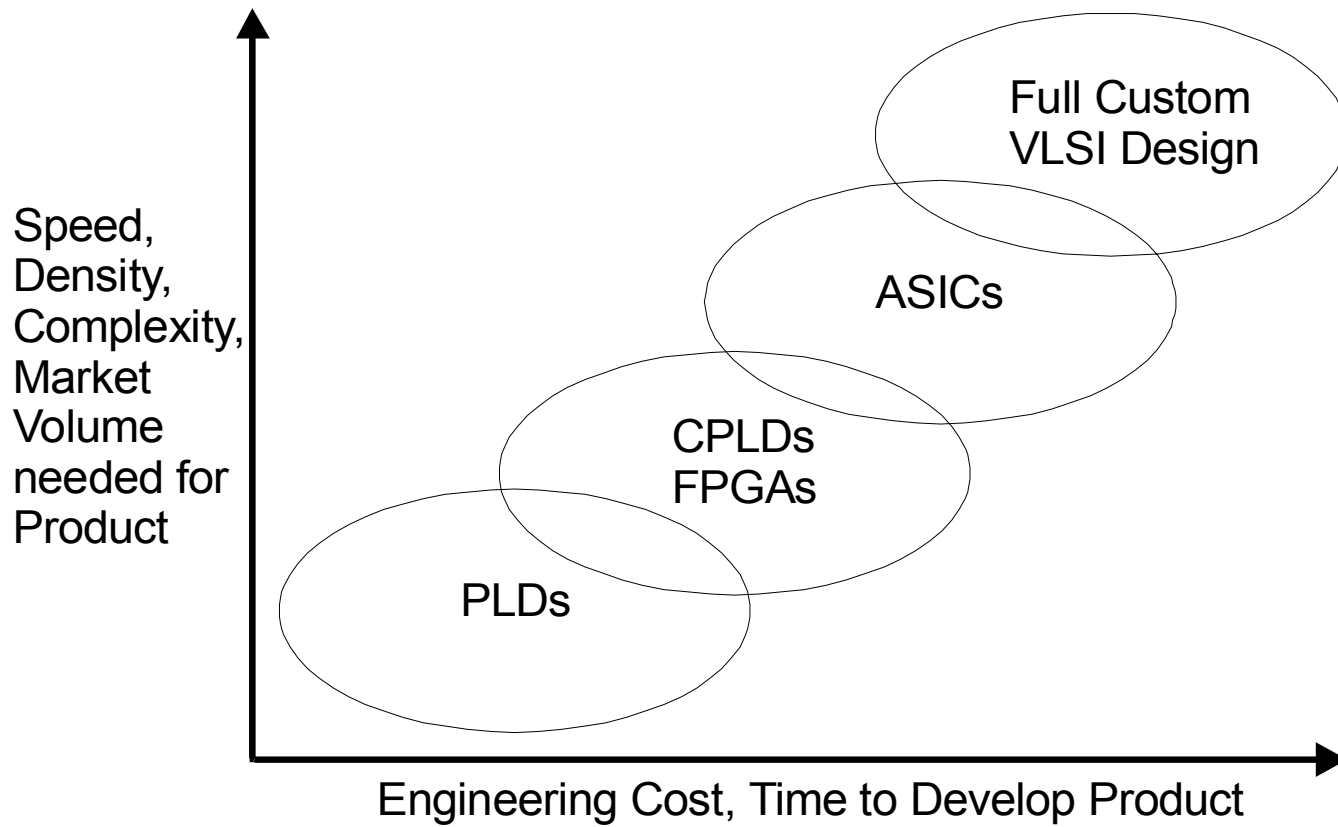


Figure 3.2 Digital logic technology tradeoffs.

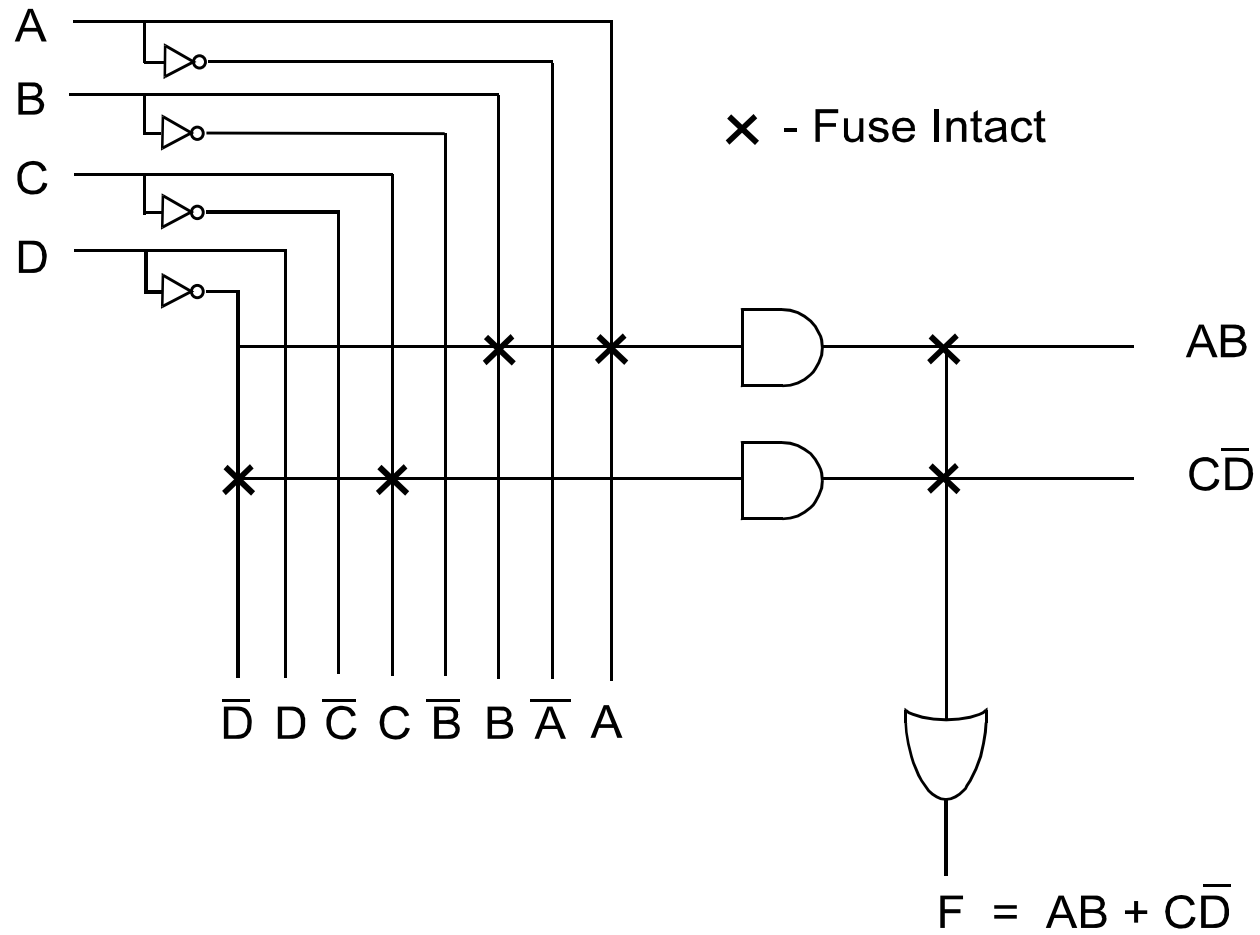


Figure 3.3 Using a PLA to implement a Sum of Products equation.



Figure 3.4 Examples of FPLDs and advanced high pin count package types.

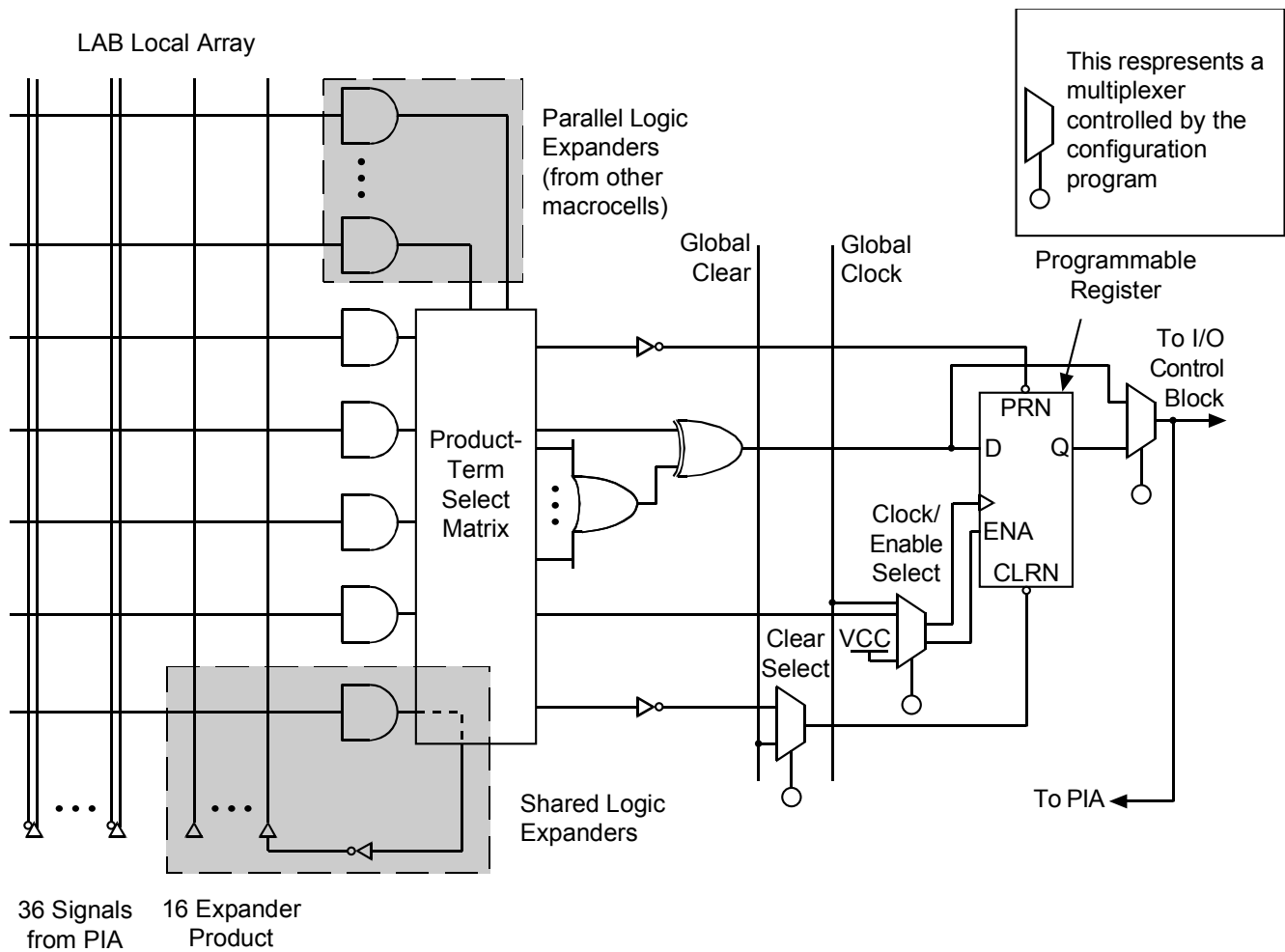


Figure 3.5 MAX 7000 macrocell.

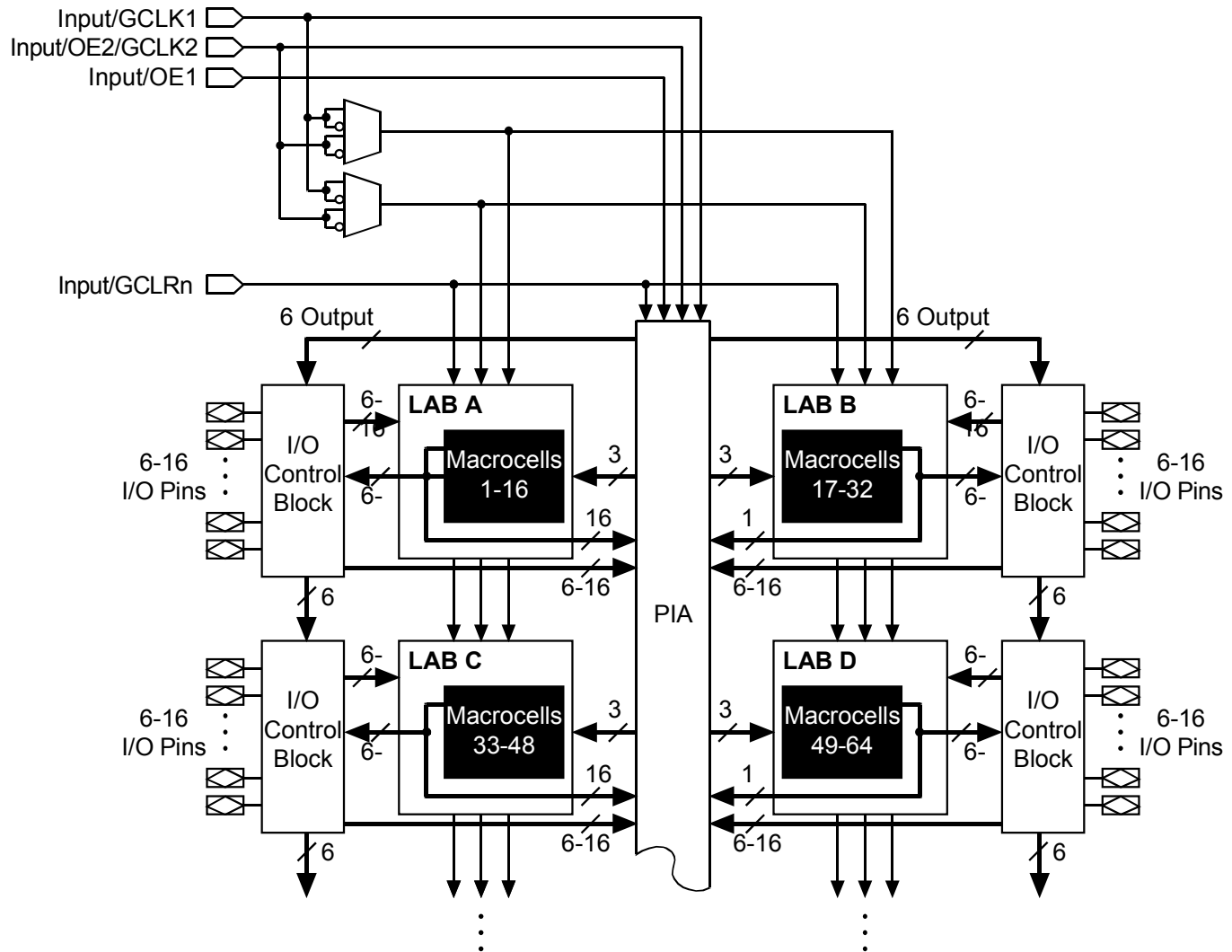


Figure 3.6 MAX 7000 CPLD architecture.

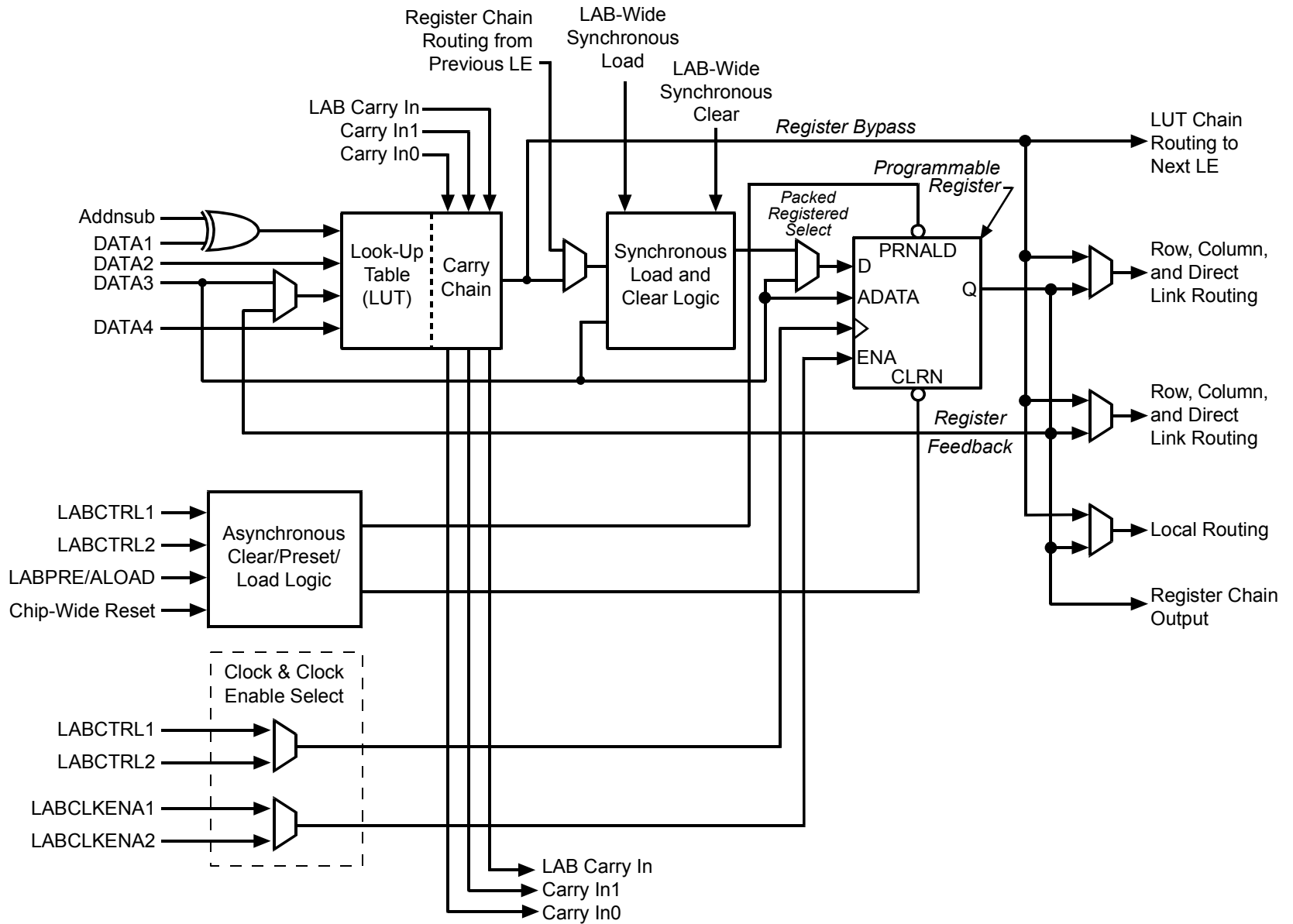


Figure 3.7 Cyclone Logic Element (LE).

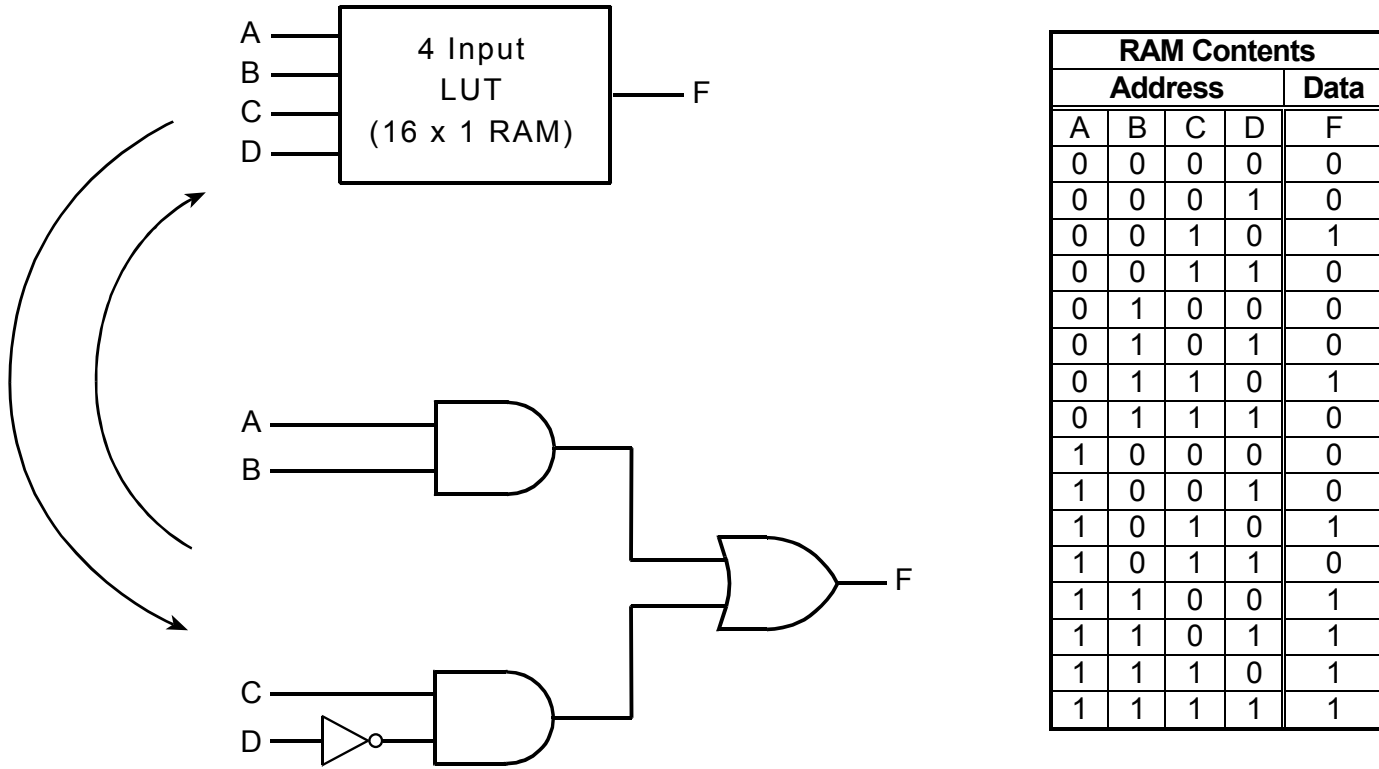


Figure 3.8 Using a lookup table (LUT) to model a gate network.

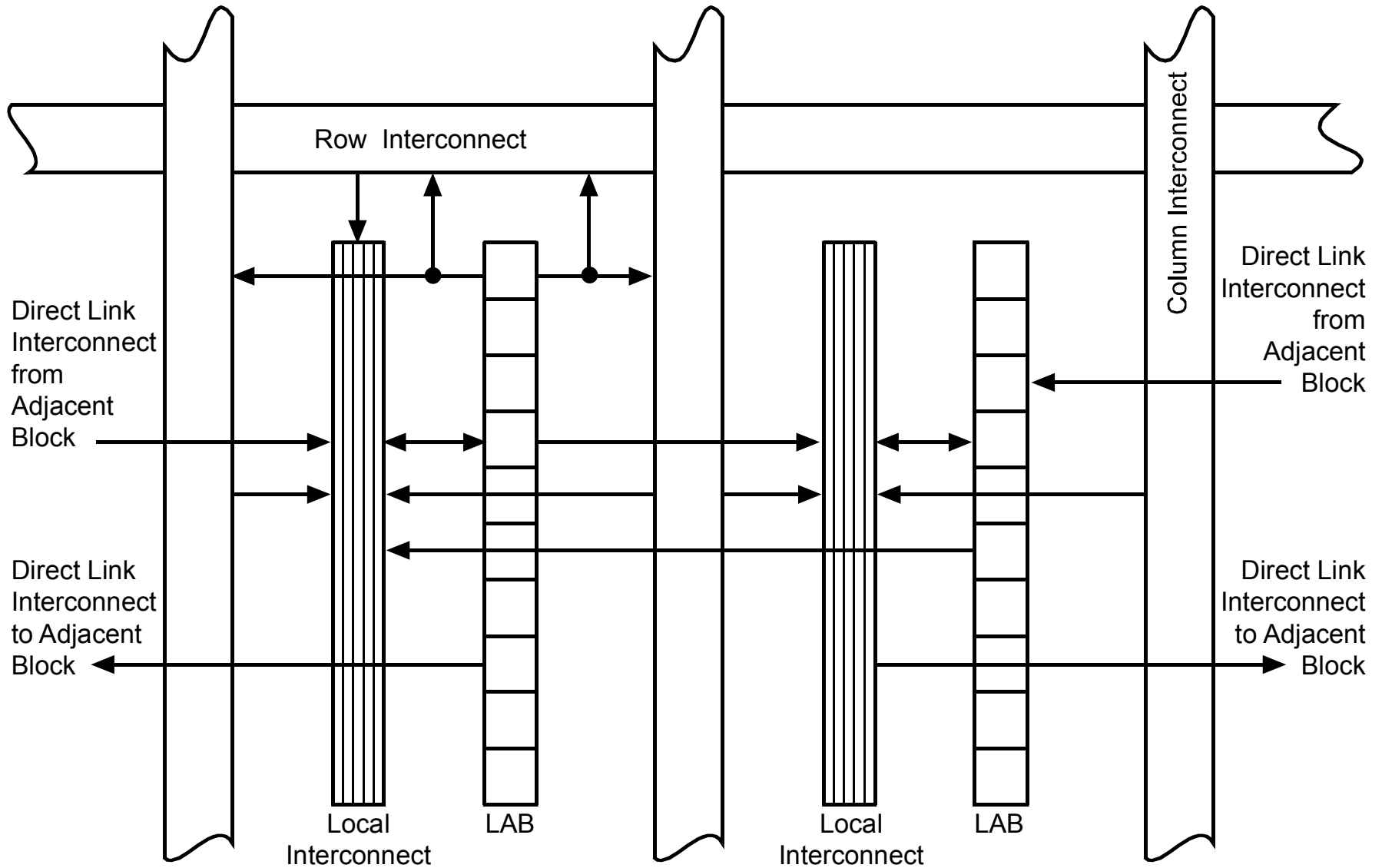


Figure 3.9 Cyclone Logic Array Blocks (LAB) and Interconnects.

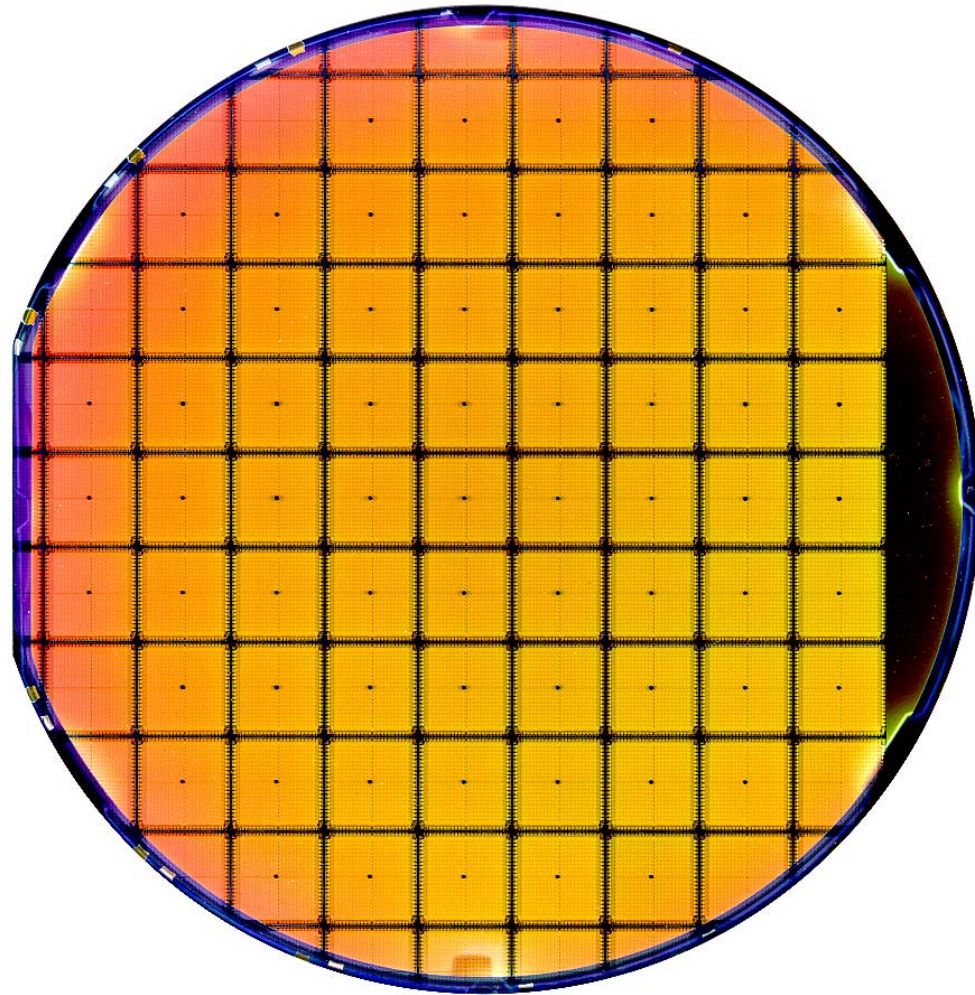


Figure 3.10 Silicon wafer containing XC4010E 10,000 gate FPGAs.

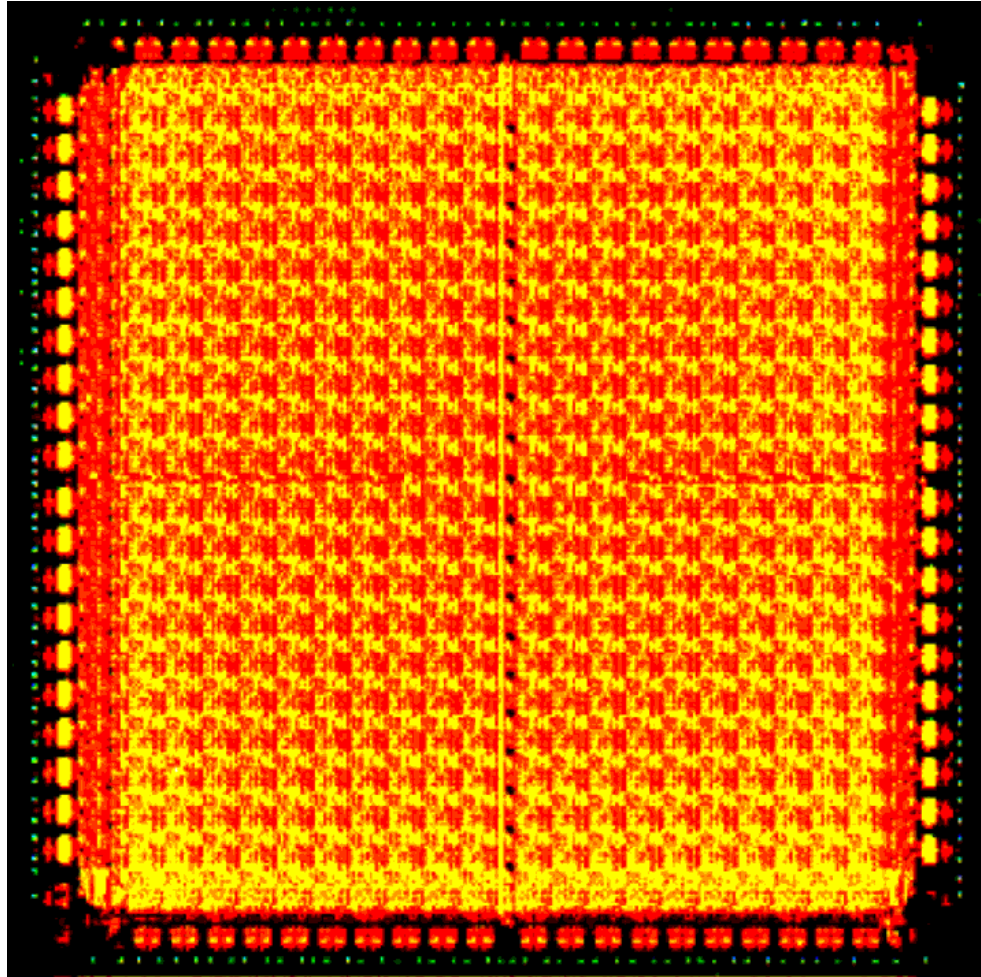


Figure 3.11 Single XC4010E FPGA die showing 20 by 20 array of logic elements and interconnect.

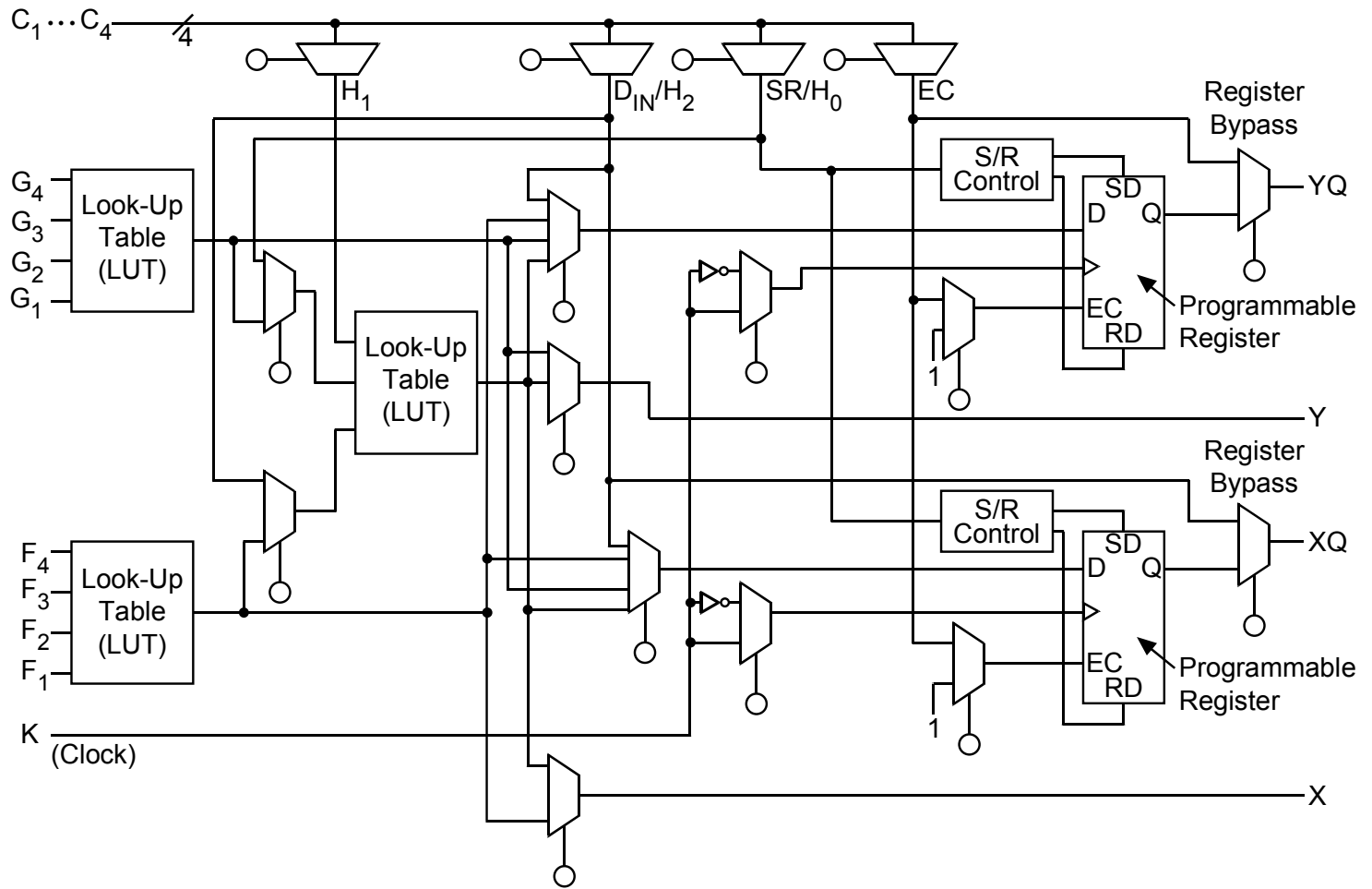


Figure 3.12 Xilinx 4000 Family Configurable Logic Block (CLB).

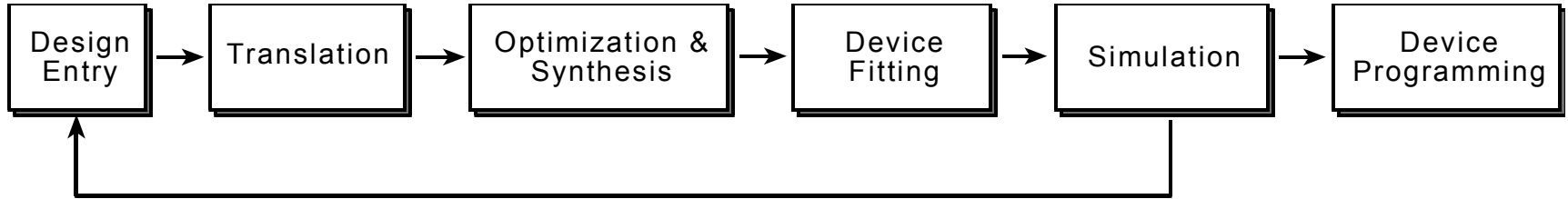


Figure 3.13 CAD tool design flow for FPLDs.