

A small SOPC-based aircraft autopilot system that contains an FPGA with a Nios processor core, a DSP processor, and memory is seen above. The bottom sensor board contains a GPS receiver, an A/D converter, MEMS gyros and accelerometers for all three axes, an airspeed sensor, and an altitude sensor. Photograph ©2004 courtesy of Henrik Christophersen, Georgia Institute of Technology Unmanned Aerial Research Facility.

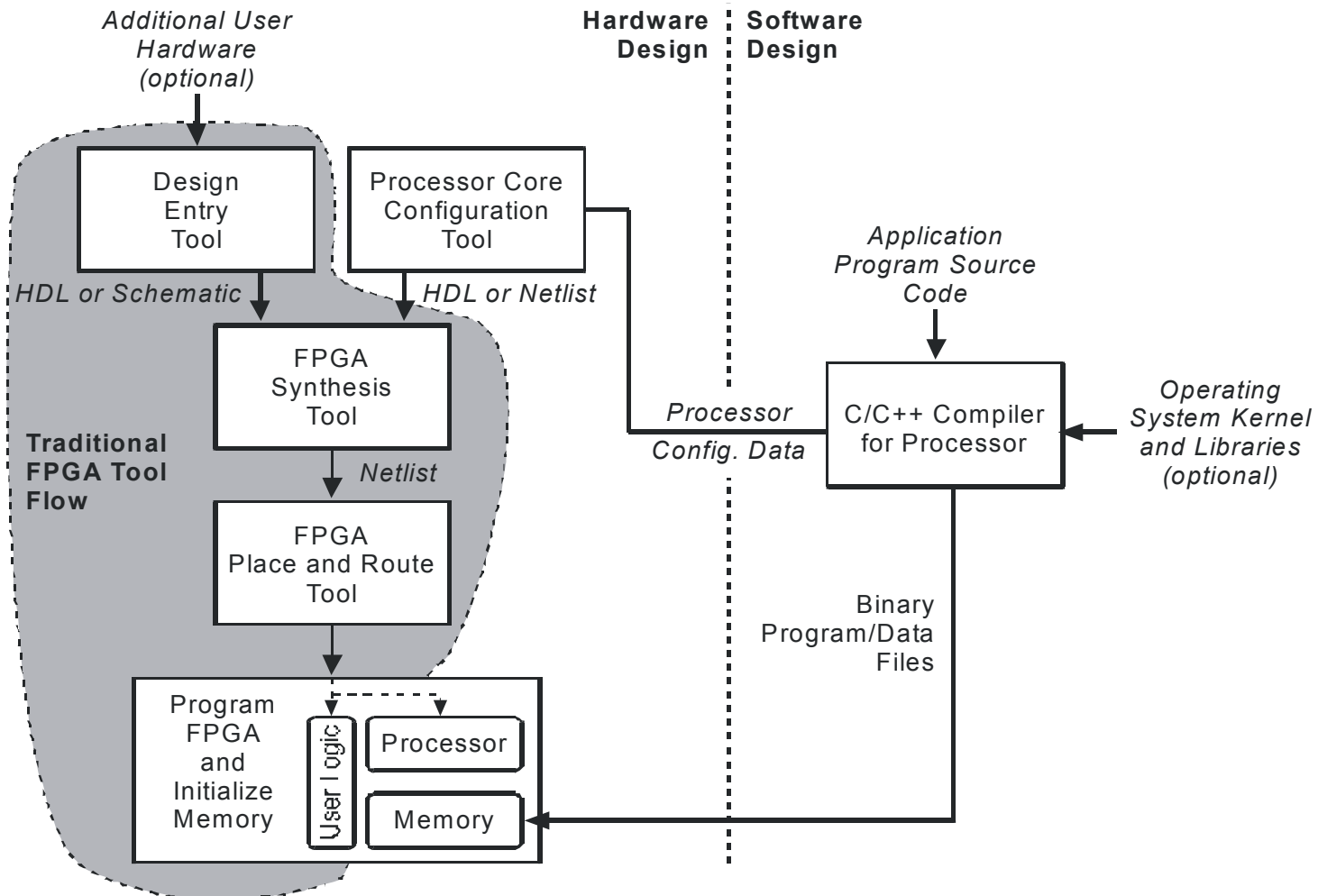
# Table 15.1 Features of Commercial Soft Processor Cores for FPGAs

Feature	Nios II 5.0	MicroBlaze 4.0
Datapath	32 bits	32 bits
Pipeline Stages	1-6	3
Frequency	Up to 200 MHz <sup>[1]</sup>	Up to 200 MHz <sup>4</sup>
Gate Count	26,000 – 72,000	30,000 – 60,000
Register File	32 general purpose & 6 special purpose	32 general purpose & 32 special purpose
Instruction Word	32 bits	32 bits
Instruction Cache	Optional	Optional
Hardware Multiply & Divide	Optional	Optional
Hardware Floating Point	Third Party	Optional

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<sup>[1]</sup> This speed is not achievable on all devices for either processor core. Some FPGAs may limit the maximum frequency to as low as 50 MHz.

**Figure 15.1** The CAD tool flow for SOPC design is comprised of the traditional design process for FPGA-based systems with the addition of the Processor Core Configuration Tool and software design tools. In this figure, the program and data memory is assumed to be on-chip for simplicity.



**Figure 15.2** This arrangement of on-chip and external memories provides flexibility and performance to an SOPC system.

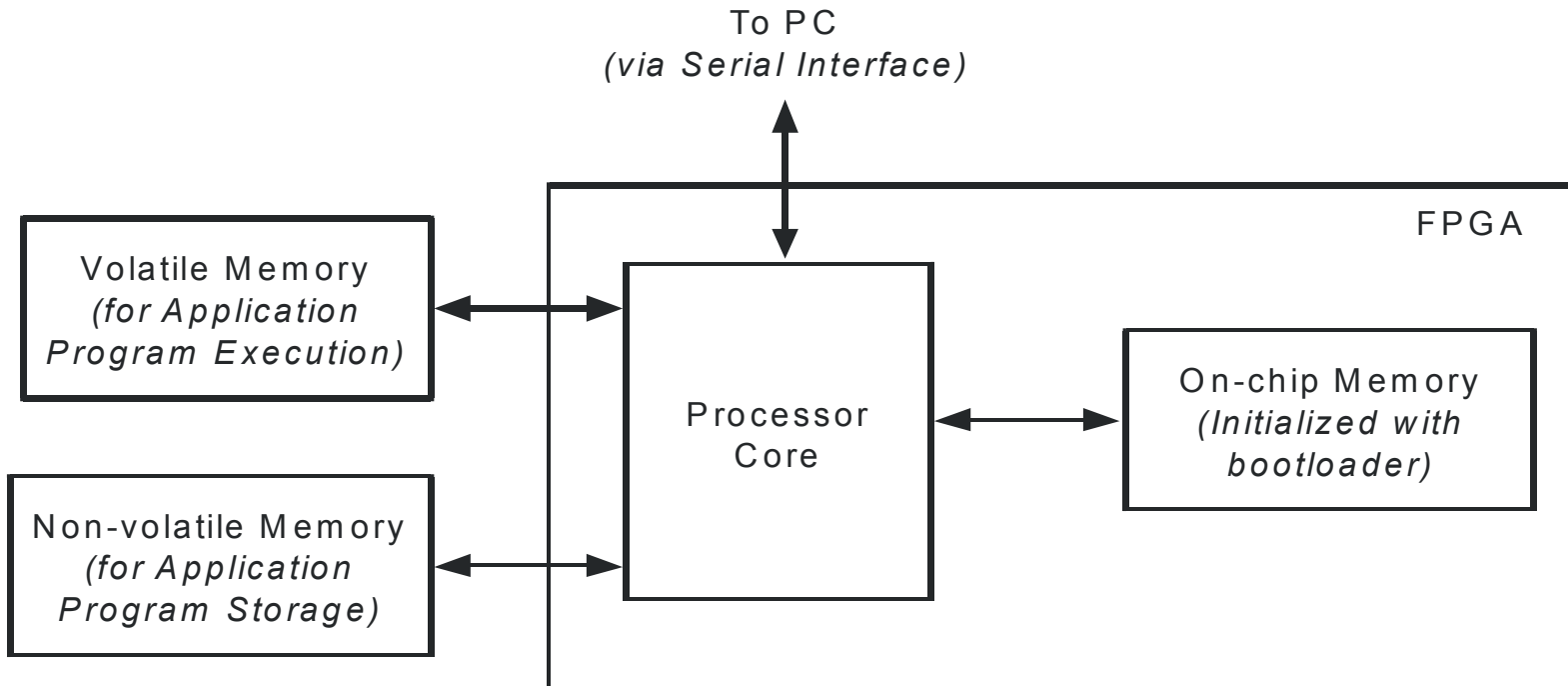


Table 15.2 Comparing SOPC, ASIC, and Fixed-Processor Design Modalities

Feature	SOPC	ASIC	Fixed-Processor
S/W Flexibility	●	●	●
H/W Flexibility	●	○	○
Reconfigurability	●	○	○
Development Time/Cost	●	○	●
Peripheral Equipment Costs	●	●	○
Performance	◐	●	●
Production Cost	◐	● <sup>[1]</sup>	●
Power Efficiency	○	●	●

Legend: ● – Good; ◐ – Moderate; ○ – Poor

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<sup>[1]</sup> In very large quantities.