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<table>
<thead>
<tr>
<th>I/O Device</th>
<th>UP 3 Pin Number Connections</th>
<th>UP 1 &amp; UP 2 Pin Number Connections</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB1</td>
<td>62 (SW7)</td>
<td>28 (FLEX PB1)</td>
</tr>
<tr>
<td>PB2</td>
<td>48 (SW4)</td>
<td>29 (FLEX PB2)</td>
</tr>
<tr>
<td>LED</td>
<td>56 (D3)</td>
<td>14 (7Seg LED DEC. PT.)</td>
</tr>
</tbody>
</table>
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module orgate (PB1, PB2, LED);

  input  PB1, PB2;
  output LED;

  // Concurrent Assignment

endmodule

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Figure 1.15 The Altera DE2 FPGA Development board