## UP3-1C6 Schematic

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NOTES:

[1] CONFIGURATION FUNCTION FOR PIN 37 IS DEFINED AS ASDo (ACTIVE SERIAL DATA OUT)

[2] nCEO PIN REMAINS UNCONNECTED BECAUSE THIS BOARD DOES NOT SUPPORT MULTIPLE FPGAs

[3] ALL THE BANKS OF EP1C6 ARE CONFIGURED FOR +3.3-V LVTTL/LVCMOS I/O STANDARD
NOTES:

[1] C2_PPT SIGNAL OF PARALLEL PORT REMAINS OPEN ON THIS BOARD (NOT CONNECTED TO ANY FPGA PIN)
   - IT IS JUST PULLED HIGH AT +5V AT PPT CONNECTOR

[2] IF +5V LOGIC LEVEL IS REQUIRED FOR V_SYNC_SHIFT & H_SYNC_SHIFT SIGNALS THEN STUFF PULL UP
   RESISTORS R367 & R558, OTHERWISE DON'T

- IT IS JUST PULLED HIGH AT +5V AT PPT CONNECTOR

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NOTES:

1. PCICLK_OUT (33.3MHz) FOR SNAP IN BOARD IS PROVIDED FROM CLOCK CHIP (PI6C106)
2. J3.34 IS USED AS A PROTO I/O ACCORDING TO THE NIOS BOARD SCHEMATICS
3. FOR LEVEL SHIFTING, SEE PAGE_10_L.S.S.C_CONN.
Note: For level shifting, see page3_ppt
NOTES:

[1] FOR LEVEL SHIFTING, SEE PAGE9_LCD DISPLAY

[2] BATTERY SOCKET IS USED FOR Li BATTERY (BT1)
NOTES:

[1] HEADER J8 => MODE SELECTION
[2] HEADER J11 => SPEED SELECTION
[3] HEADER J9 => HIGH SPEED
[4] HEADER J10 => LOW SPEED
SERIAL PORT (FULL MODEM)

- **TX_OUT**: 28
- **DTR_OUT**: 24
- **RTS_OUT**: 2
- **RI_IN**: 9
- **CD_IN**: 27
- **RX_IN**: 21
- **RTS_OUT_FPGA**: 13
- **DTR_OUT_FPGA**: 10
- **RI_IN_FPGA**: 12
- **CD_IN_FPGA**: 11
- **RX_IN_FPGA**: 10
- **RSIN4**: 16
- **RSIN5**: 15
- **Q2**: mmt2407
- **D15**: LED
- **R174**: 220
- **C83**: 0.1uF
- **C87**: 0.1uF

**Components**
- **U21**: MAX 3243
NOTE: FOR LEVEL SHIFTING, SEE PAGE3_PPT
NOTES:

[1] RESET TIME Td = 2.6 x 10E4 (Ct)

[2] FOR LEVEL SHIFTING, SEE PAGE 9 LCD_DISPLAY
NOTES:
[1] BY SELECTING HIGH OR LOW INPUT THROUGH J7, 100 MHz OR 66.6 MHz CAN BE SELECTED RESPECTIVELY
[2] 12pF CAPACITORS ARE USED AS EMI REDUCING CAPACITORS
[3] STUFFING OPTIONS FOR SPREAD INPUT:
STUFFED R374 - DEFAULT HIGH
STUFFED R375 - ENABLE SPREAD#
NOTES:

[1] R158 IS NOT STUFFED (WP PIN IS KEPT FLOATING) FOR NORMAL OPERATIONS
   - STUFF R158 TO ENABLE WRITE PROTECTION IN THE SUPPORTED DEVICE

NOTES:

[1] HERE FOUR USER DEFINABLE PUSH BUTTON SWITCHES ARE SHOWN

[2] THE PUSH BUTTON SWITCH FOR SYSTEM RESET IS SEPARATELY DEFINED ON PAGE 16 (RESET CIRCUIT)

[3] BE CAREFUL WHEN MOUNTING THE DIP SWITCH
BYTE BLASTER II 10 PIN MALE HEADER FOR AS MODE [DCLK(FPGA) => DCLK(CONFIG. PROM)]

BYTE BLASTER II 10 PIN MALE HEADER FOR JTAG CONFIGURATION

CONFIGURATION PROM