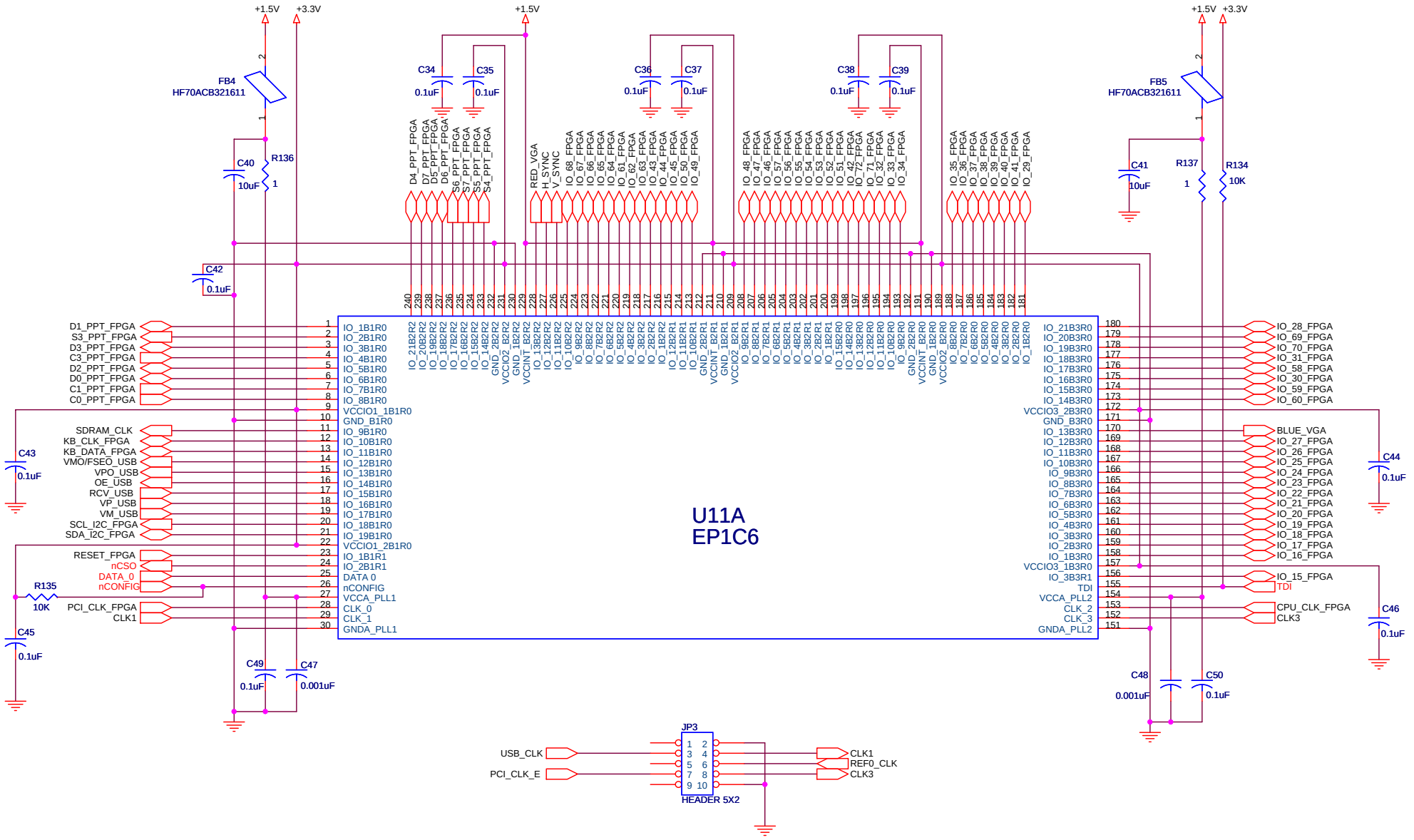
UP3-1C6 Schematic


U11A
EP1C6
FB4
HF70ACB321611
FB5
HF70ACB321611
+1.5V
+3.3V
C34
C35
C36
C37
C38
C39
C40
C41
C42
C43
C44
C45
C46
C47
C48
C49
C50
0.1uF
10uF
0.001uF
R136
R137
R134
R135
10K
1
D4_PPT_FPGA
D7_PPT_FPGA
D5_PPT_FPGA
D6_PPT_FPGA
S6_PPT_FPGA
S7_PPT_FPGA
S5_PPT_FPGA
S4_PPT_FPGA
RED_VGA
H_SYNC
V_SYNC
IO_68_FPGA
IO_67_FPGA
IO_66_FPGA
IO_65_FPGA
IO_64_FPGA
IO_61_FPGA
IO_62_FPGA
IO_63_FPGA
IO_43_FPGA
IO_44_FPGA
IO_45_FPGA
IO_50_FPGA
IO_49_FPGA
IO_48_FPGA
IO_47_FPGA
IO_46_FPGA
IO_57_FPGA
IO_56_FPGA
IO_55_FPGA
IO_54_FPGA
IO_53_FPGA
IO_52_FPGA
IO_51_FPGA
IO_42_FPGA
IO_71_FPGA
IO_32_FPGA
IO_33_FPGA
IO_34_FPGA
IO_35_FPGA
IO_36_FPGA
IO_37_FPGA
IO_38_FPGA
IO_39_FPGA
IO_40_FPGA
IO_41_FPGA
IO_29_FPGA
D1_PPT_FPGA
S3_PPT_FPGA
D3_PPT_FPGA
C3_PPT_FPGA
D2_PPT_FPGA
D0_PPT_FPGA
C1_PPT_FPGA
C0_PPT_FPGA
SDRAM_CLK
KB_CLK_FPGA
KB_DATA_FPGA
VMO/FSEO_USB
VPO_USB
OE_USB
RCV_USB
VP_USB
VM_USB
SCL_I2C_FPGA
SDA_I2C_FPGA
RESET_FPGA
nCSO
DATA_0
nCONFIG
PCI_CLK_FPGA
CLK1
IO_28_FPGA
IO_69_FPGA
IO_70_FPGA
IO_31_FPGA
IO_58_FPGA
IO_30_FPGA
IO_59_FPGA
IO_60_FPGA
BLUE_VGA
IO_27_FPGA
IO_26_FPGA
IO_25_FPGA
IO_24_FPGA
IO_23_FPGA
IO_22_FPGA
IO_21_FPGA
IO_20_FPGA
IO_19_FPGA
IO_18_FPGA
IO_17_FPGA
IO_16_FPGA
IO_15_FPGA
TDI
CPU_CLK_FPGA
CLK3
JP3
HEADER 5X2
USB_CLK
PCI_CLK_E
CLK1
REF0_CLK
CLK3
EP1C6 CYCLONE FPGA
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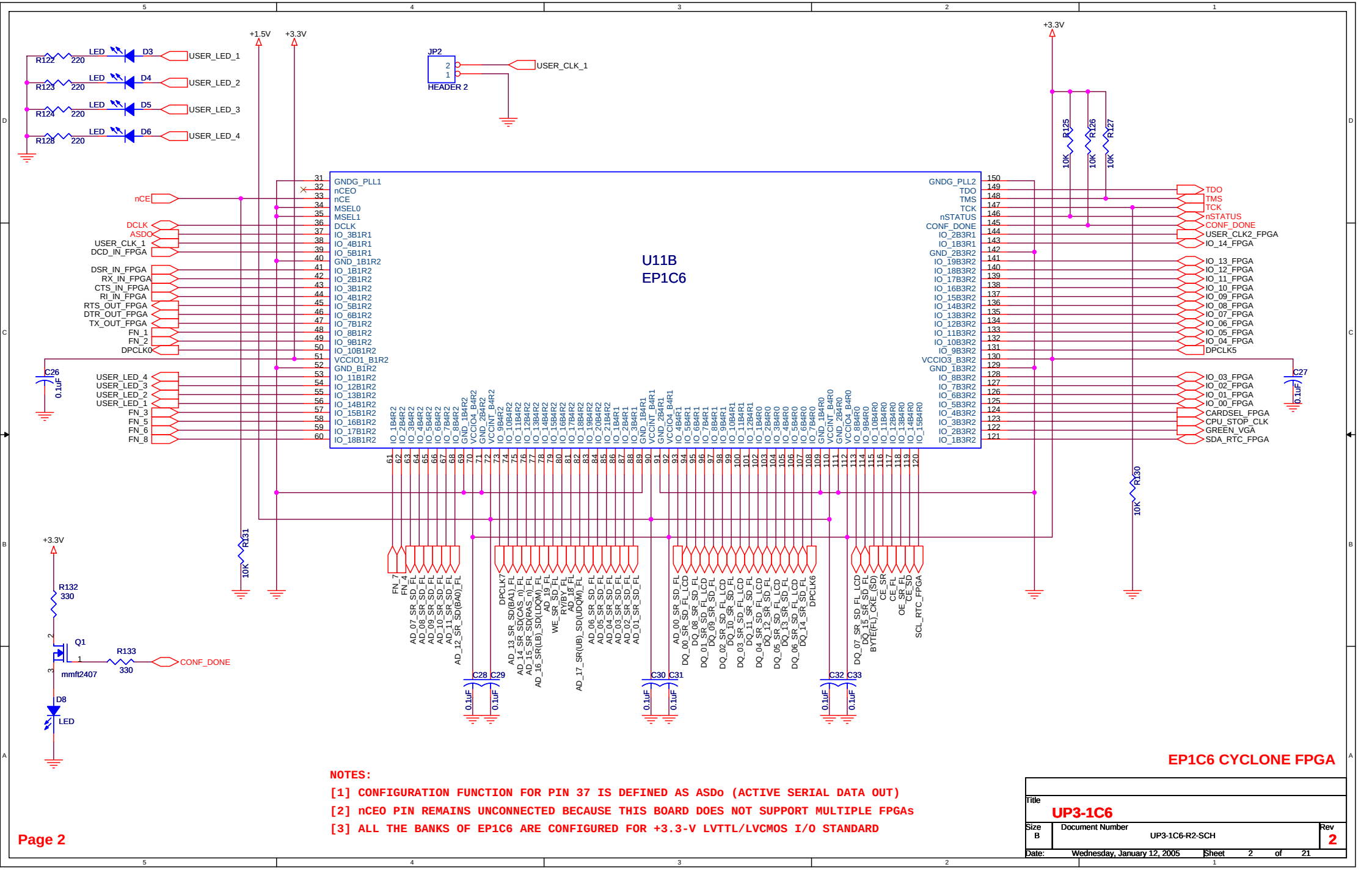
21



NOTES:

[1] CONFIGURATION FUNCTION FOR PIN 37 IS DEFINED AS ASDo (ACTIVE SERIAL DATA OUT)

[2] nCEO PIN REMAINS UNCONNECTED BECAUSE THIS BOARD DOES NOT SUPPORT MULTIPLE FPGAs

[3] ALL THE BANKS OF EP1C6 ARE CONFIGURED FOR +3.3-V LVTTL/LVCMOS I/O STANDARD

EP1C6 CYCLONE FPGA

Page 2

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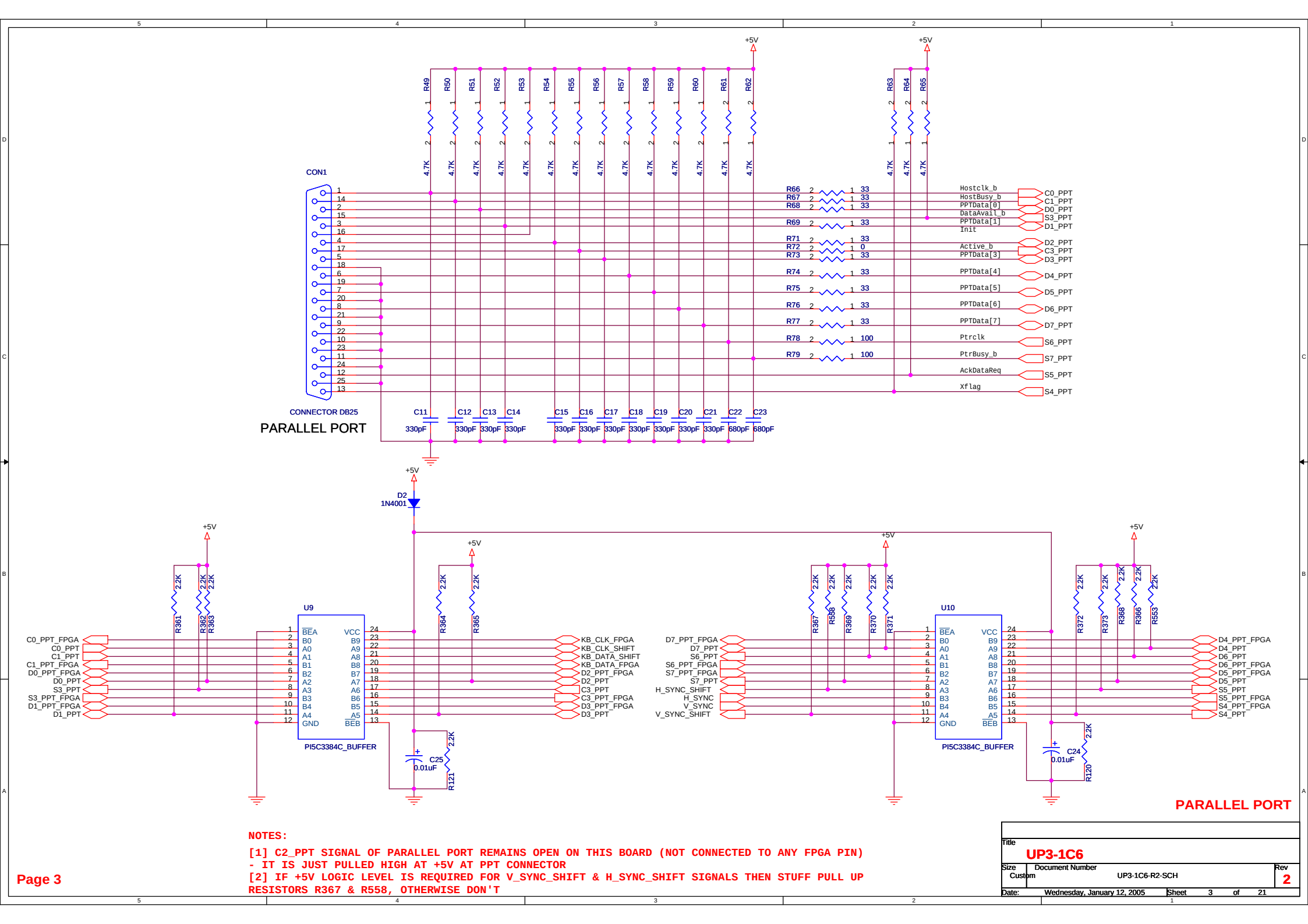

PARALLEL PORT

NOTES:

[1] C2_PPT SIGNAL OF PARALLEL PORT REMAINS OPEN ON THIS BOARD (NOT CONNECTED TO ANY FPGA PIN) - IT IS JUST PULLED HIGH AT +5V AT PPT CONNECTOR

[2] IF +5V LOGIC LEVEL IS REQUIRED FOR V_SYNC_SHIFT & H_SYNC_SHIFT SIGNALS THEN STUFF PULL UP RESISTORS R367 & R558, OTHERWISE DON'T

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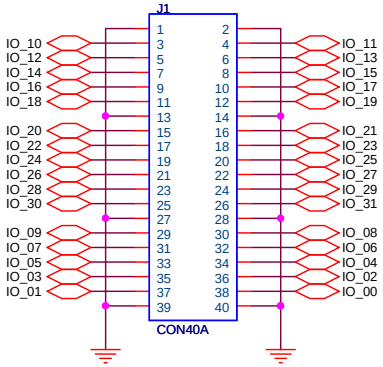

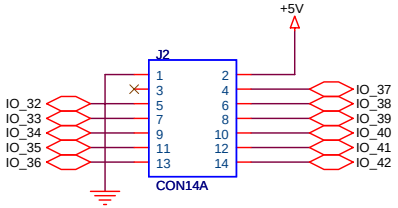

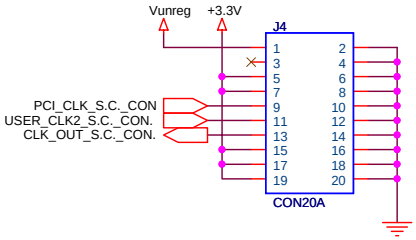

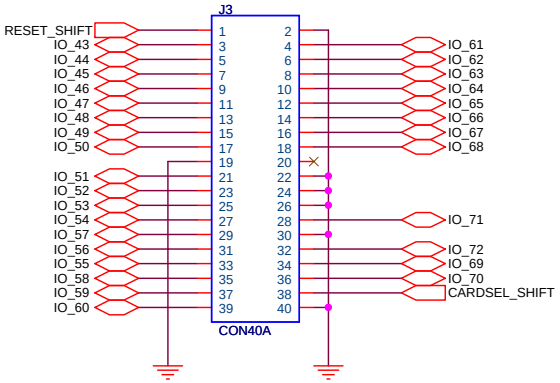

NOTES:

[1] PCICLK_OUT (33.3MHz) FOR SNAP IN BOARD IS PROVIDED FROM CLOCK CHIP (PI6C106)

[2] J3.34 IS USED AS A PROTO I/O ACCORDING TO THE NIOS BOARD SCHEMATICS

[3] FOR LEVEL SHIFTING, SEE PAGE_10_L.S.S.C.CONN.

SANTA CRUZ CONNECTOR

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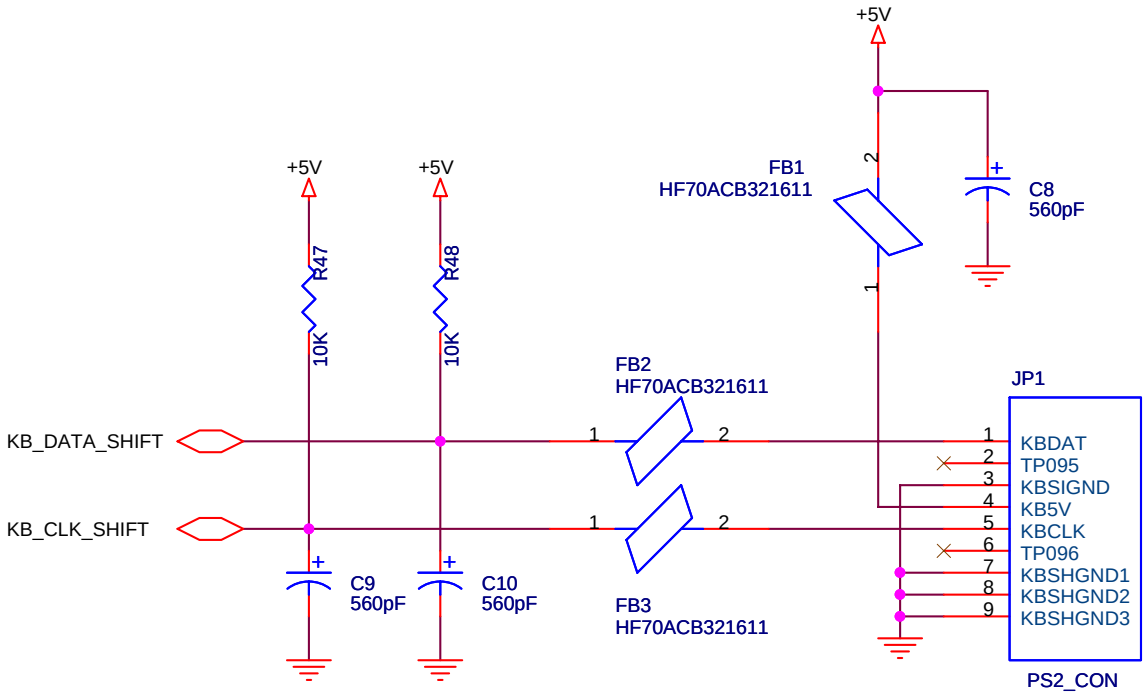

NOTE: FOR LEVEL SHIFTING, SEE PAGE3_PPT

PS/2 CONNECTOR

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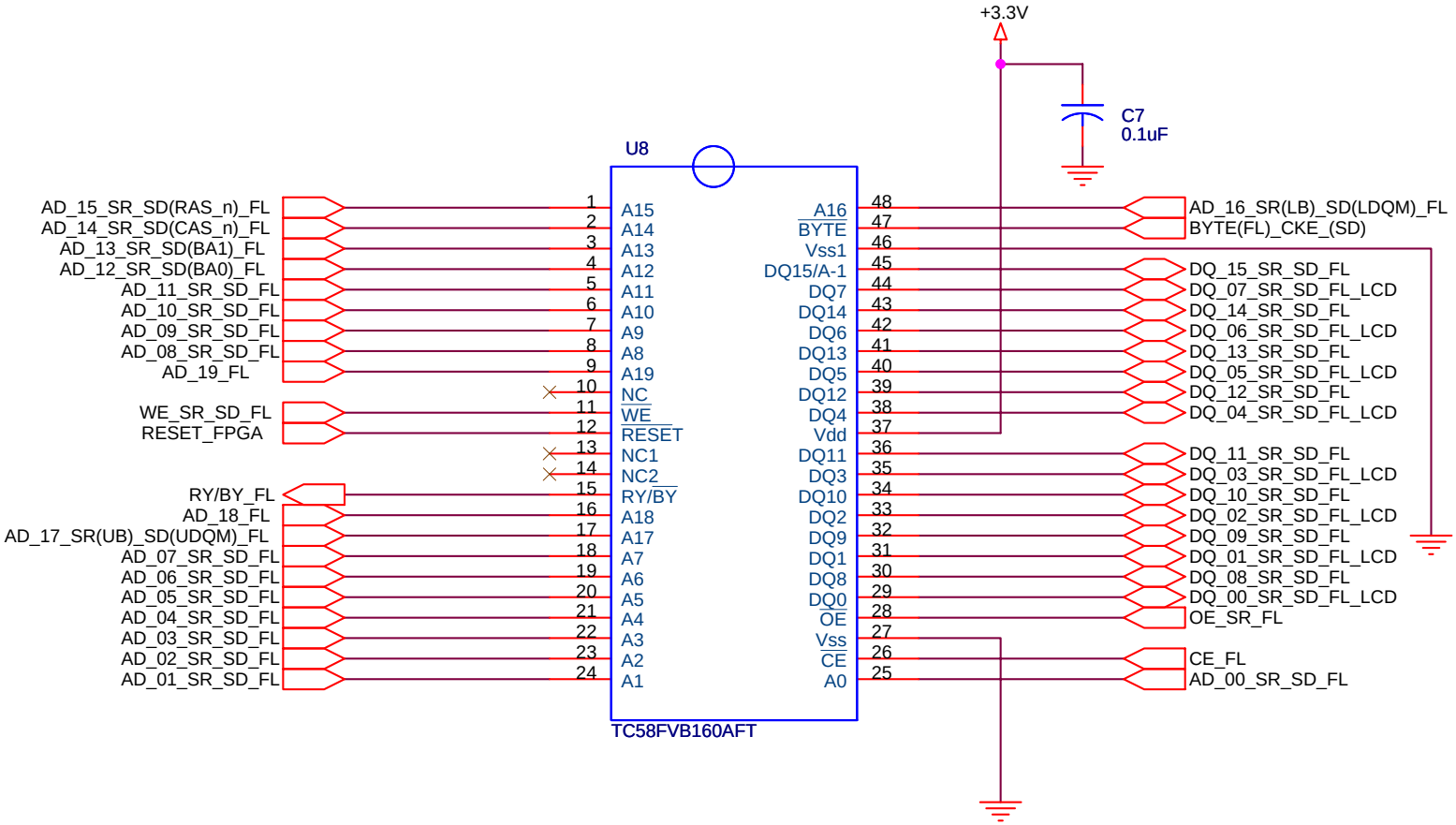

CMOS FLASH

Page 6

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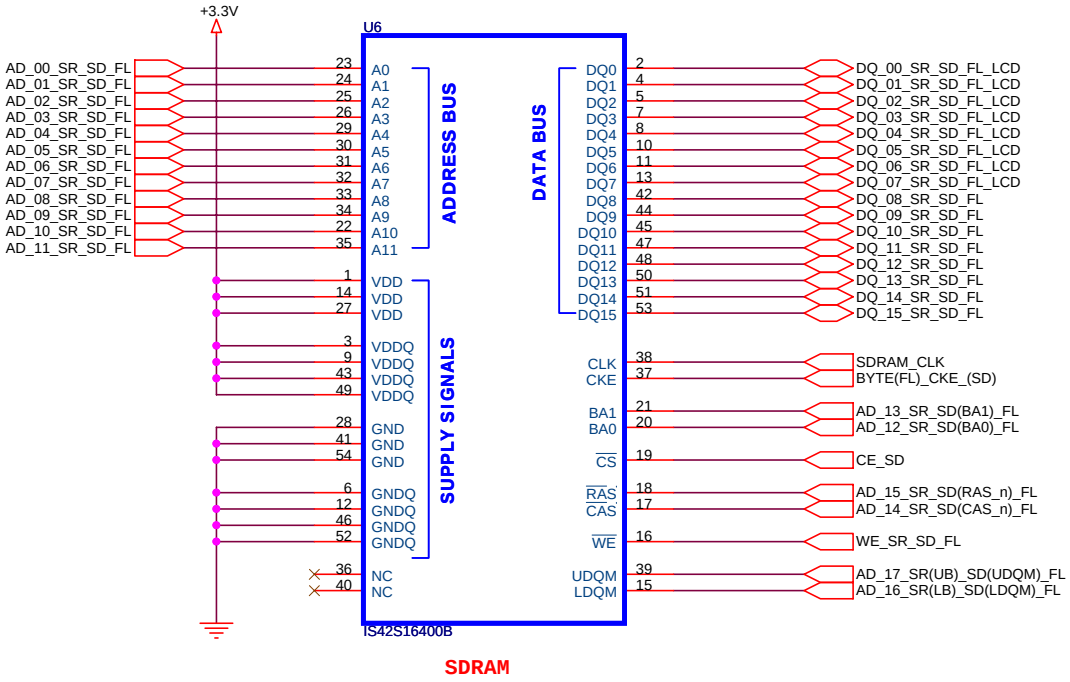
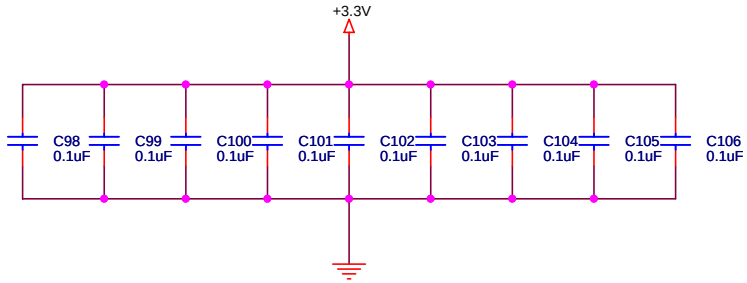


SDRAM



DECOUPLING CAPS

CMOS SDRAM

Title: UP3-1C6		
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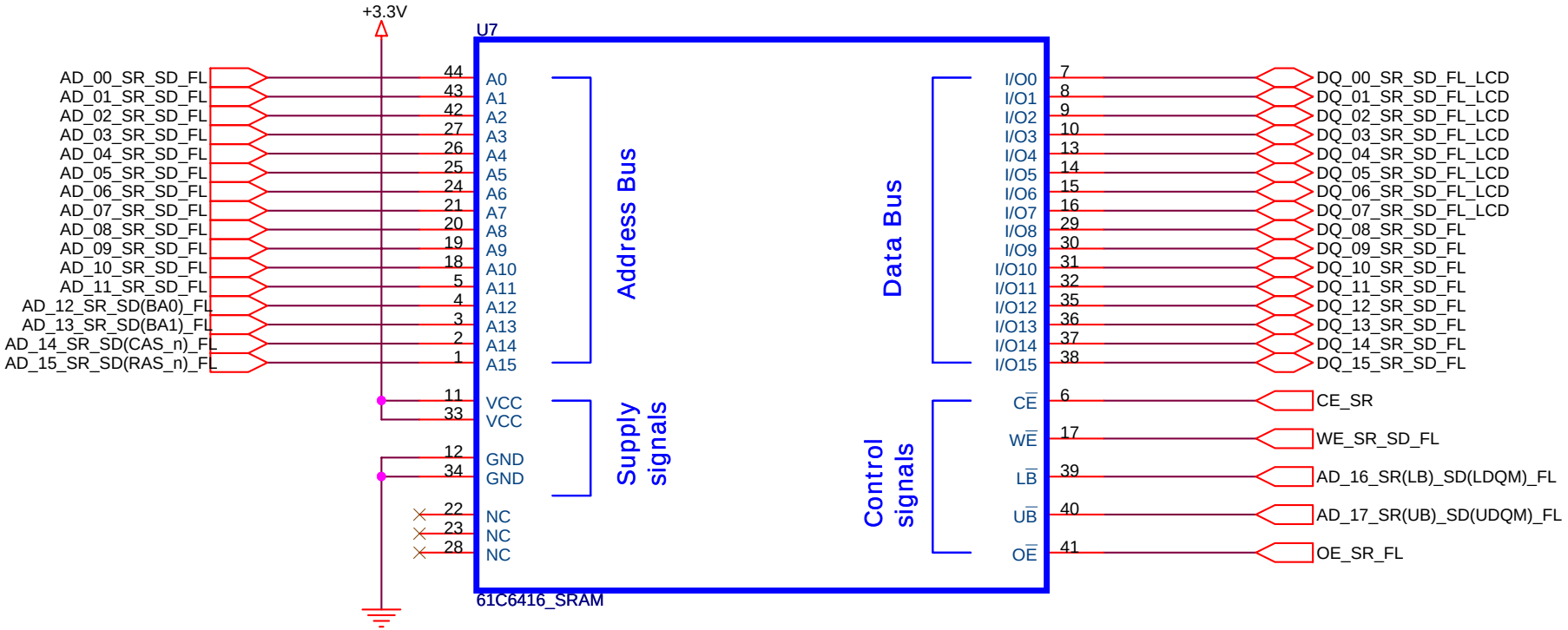

SRAM

SRAM

PAGE 8

Title: UP3-1C6		
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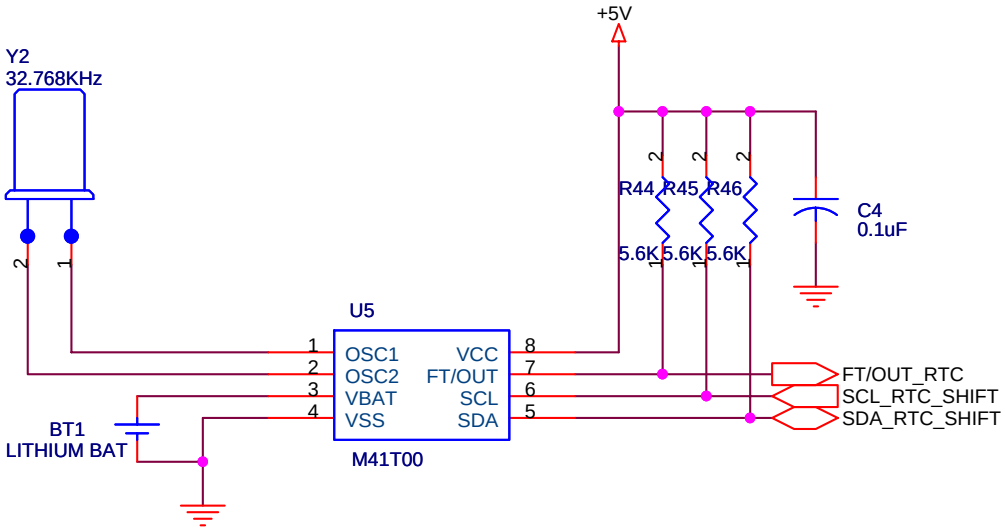

NOTES:

[1] FOR LEVEL SHIFTING, SEE PAGE9_LCD DISPLAY

[2] BATTERY SOCKET IS USED FOR Li BATTERY (BT1)

I2C RTC

Title: **UP3-1C6**		
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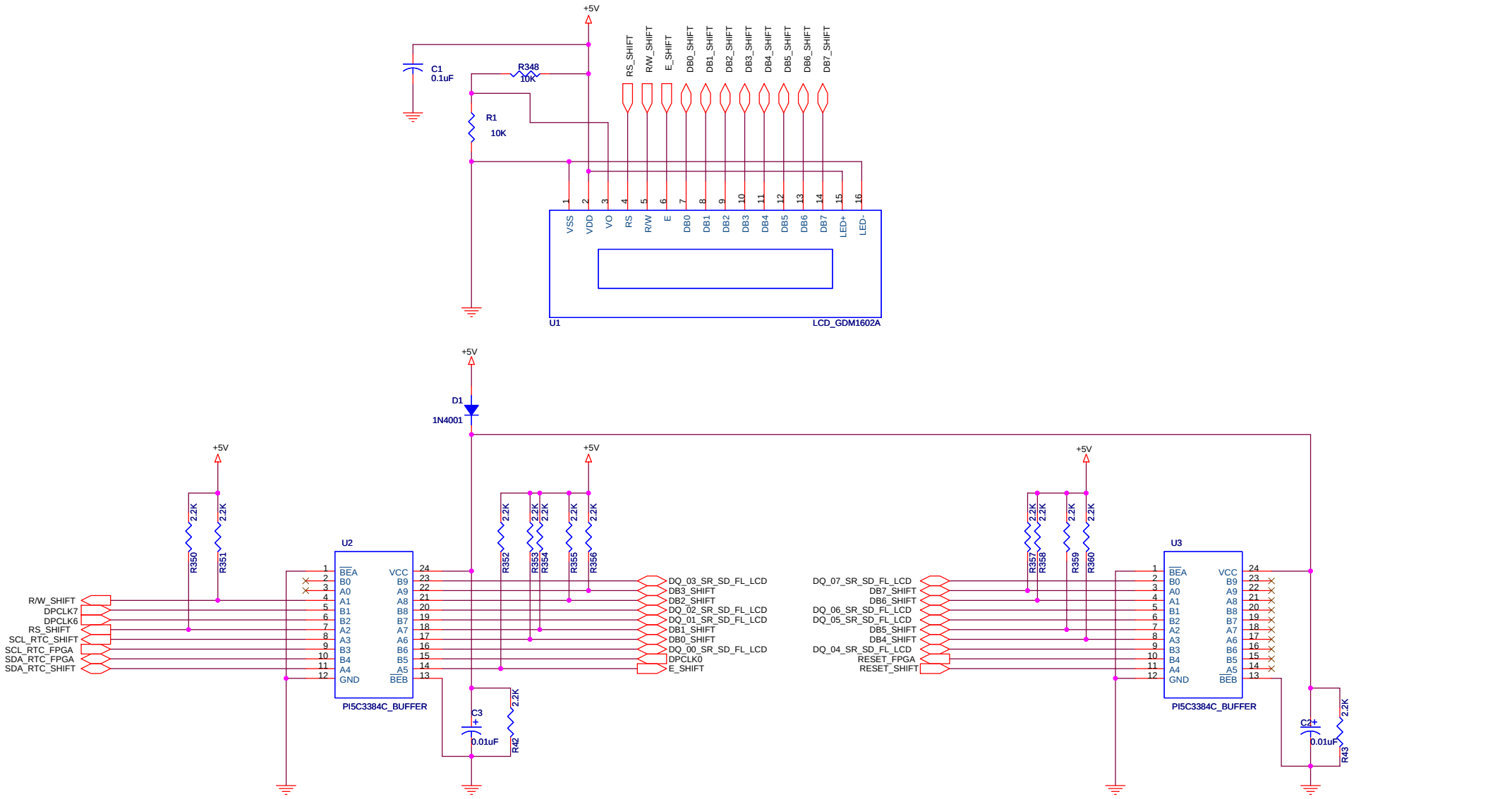

LCD DISPLAY

Page 10

Title	UP3-1C6	
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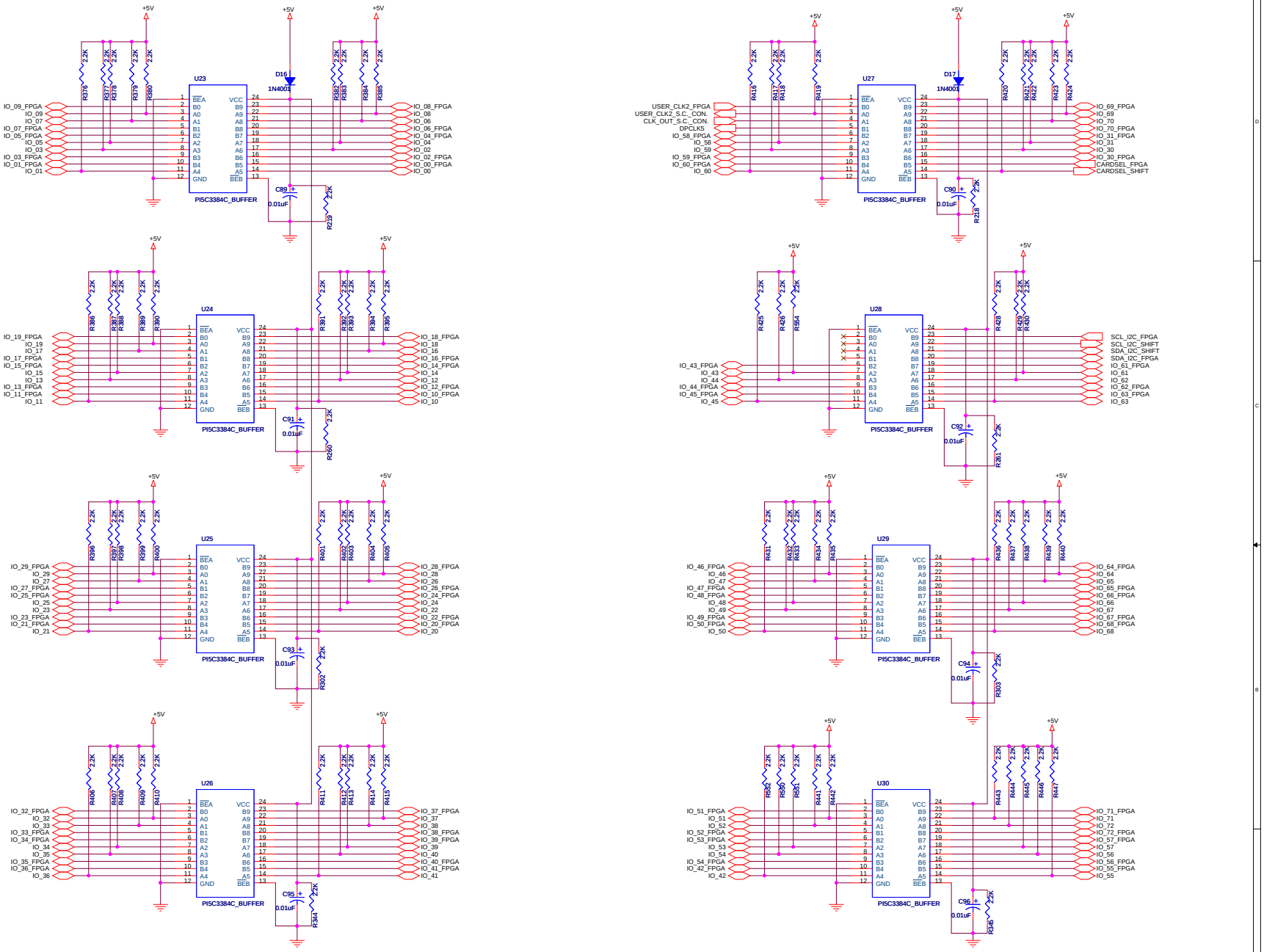

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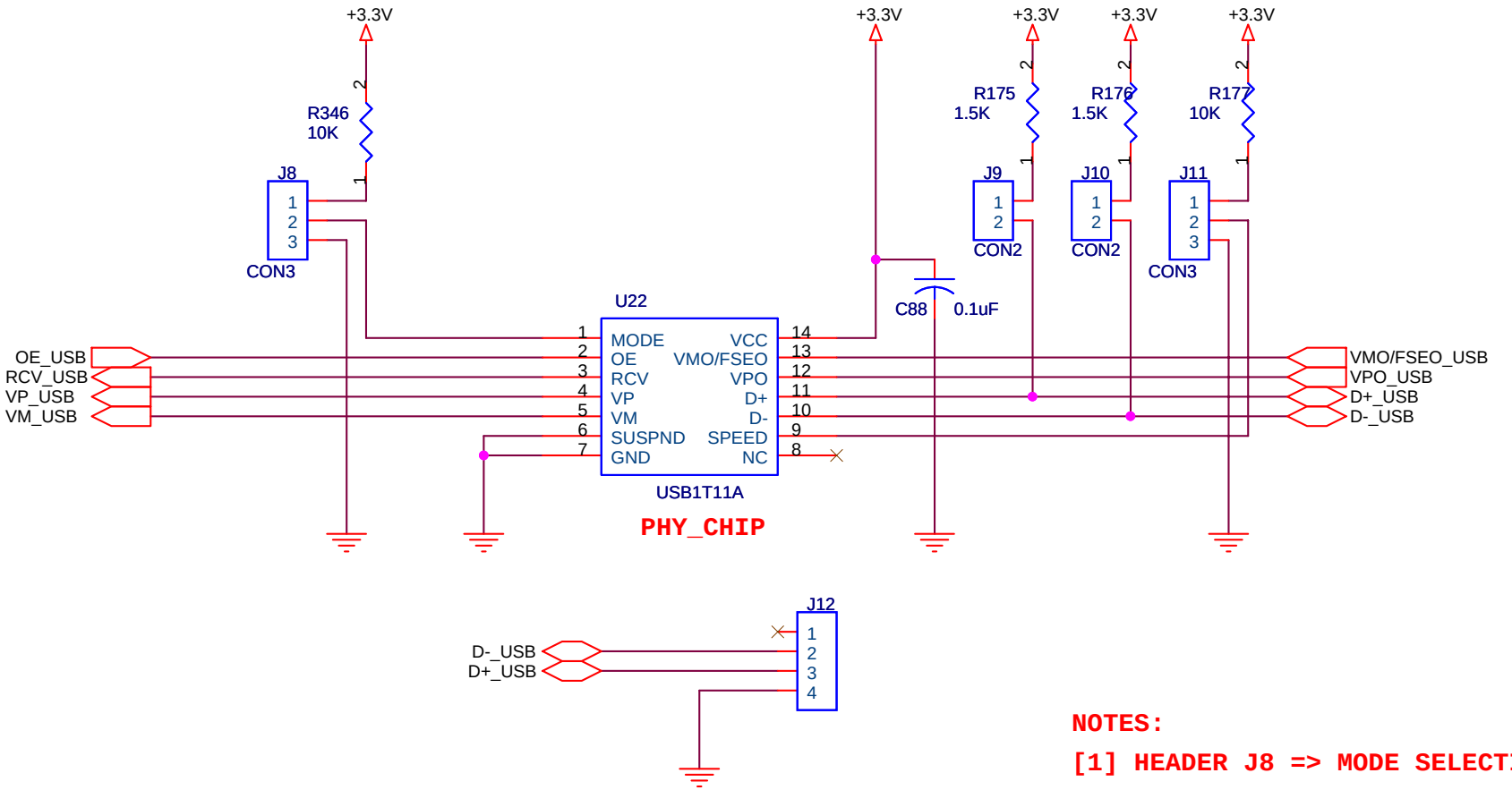

PHY_CHIP

USB_B_TYPE_CONNECTOR

NOTES:

[1] HEADER J8 => MODE SELECTION

[2] HEADER J11 => SPEED SELECTION

[3] HEADER J9 => HIGH SPEED

[4] HEADER J10 => LOW SPEED

USB PHY CHIP AND USB B-TYPE CONNECTOR

Title: **UP3-1C6**		
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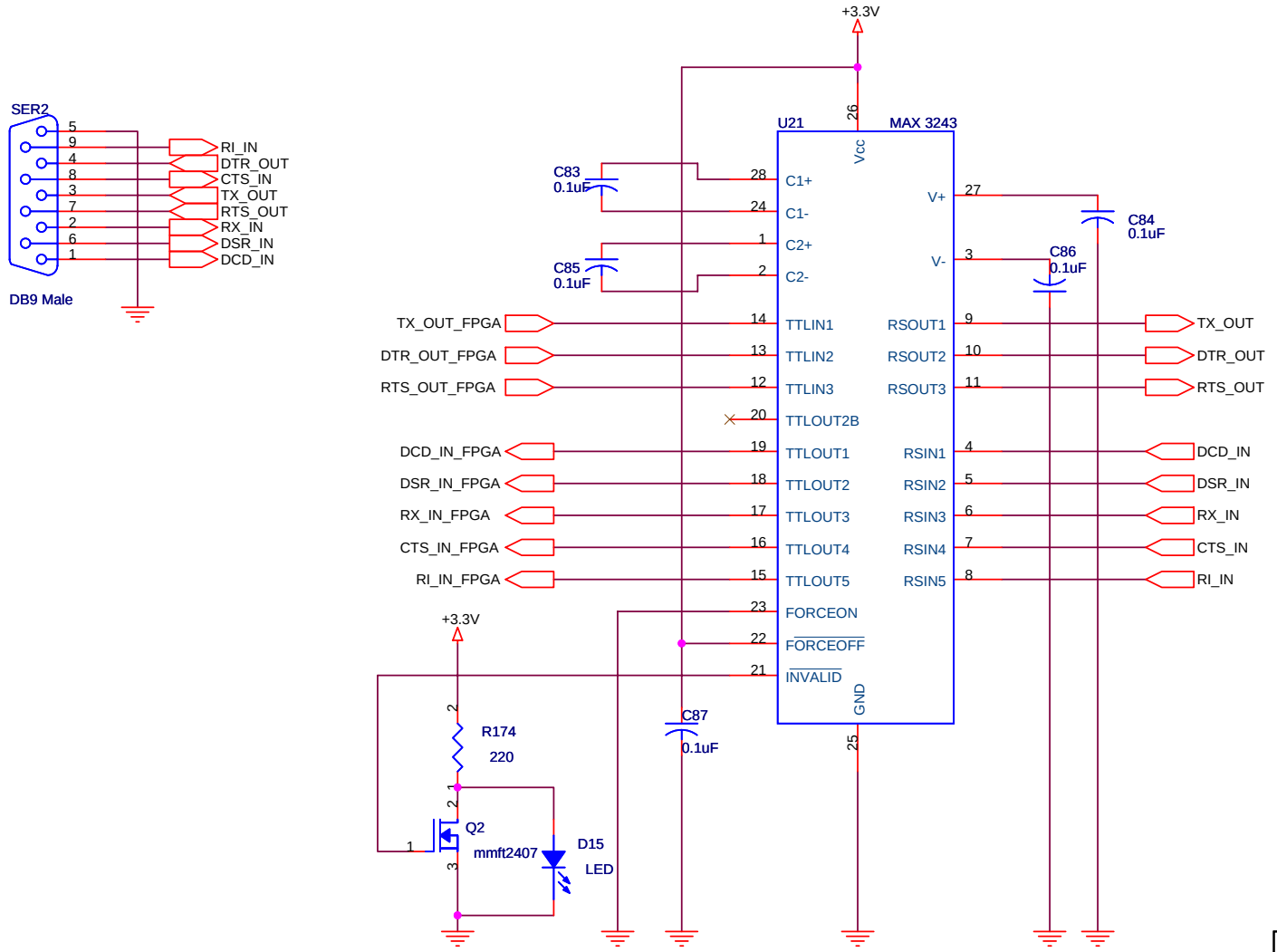

SERIAL PORT (FULL MODEM)

Title: UP3-1C6		
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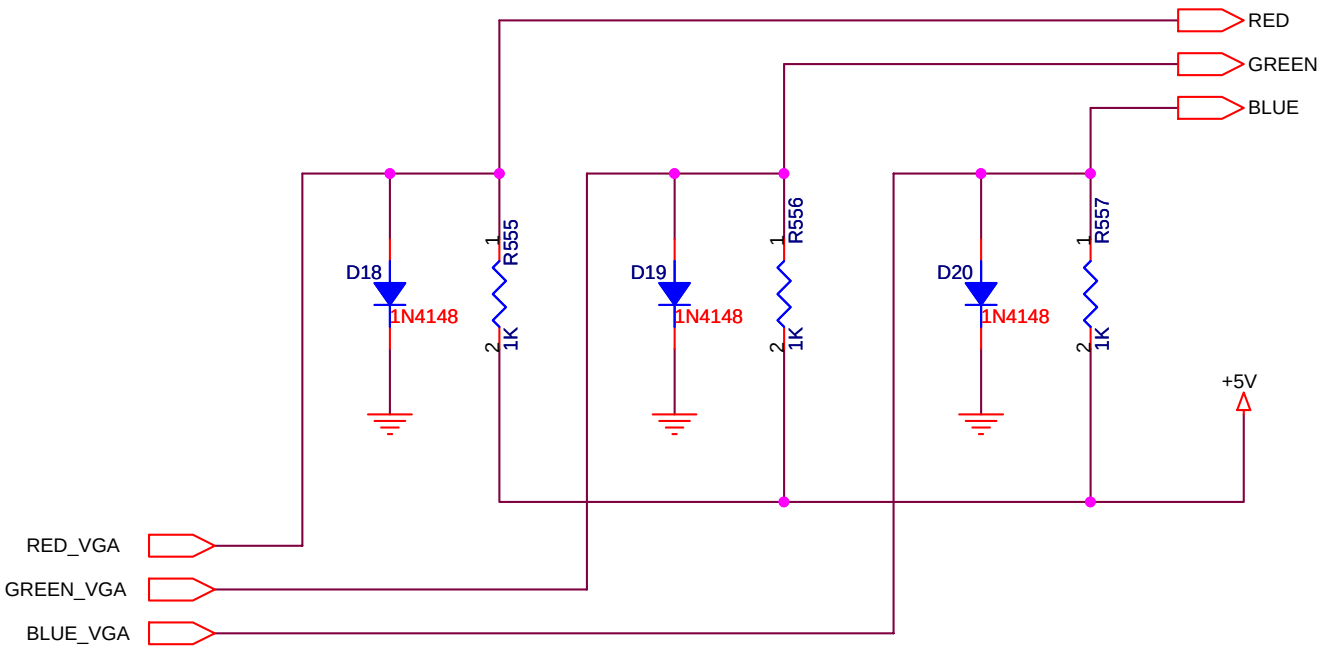

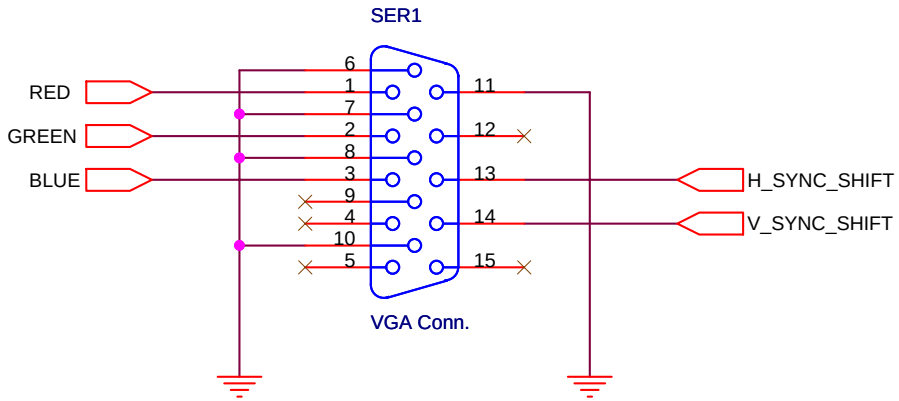

VGA INTERFACE

NOTE: FOR LEVEL SHIFTING, SEE PAGE3_PPT

Title: UP3-1C6		
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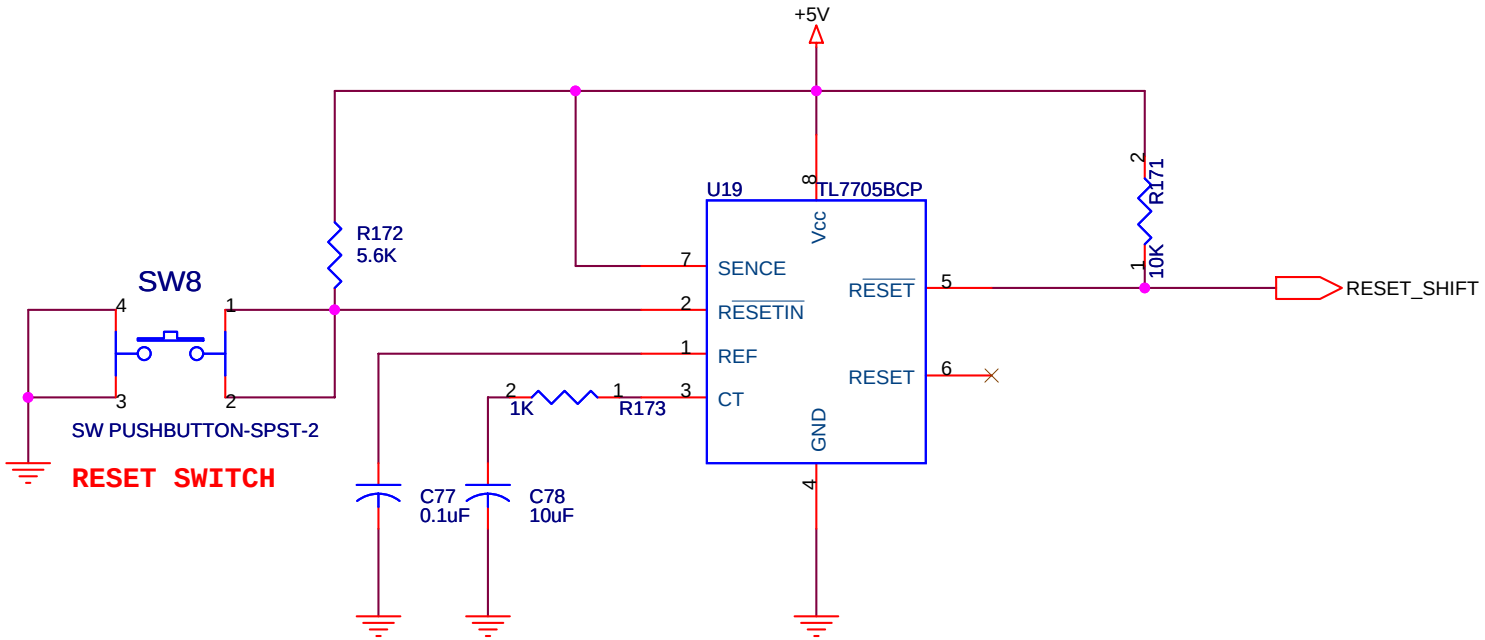

NOTES:

[1] RESET TIME Td = 2.6 x 10E4 (Ct)

[2] FOR LEVEL SHIFTING, SEE PAGE 9 LCD_DESPLAY

RESET CIRCUIT

Title: UP3-1C6		
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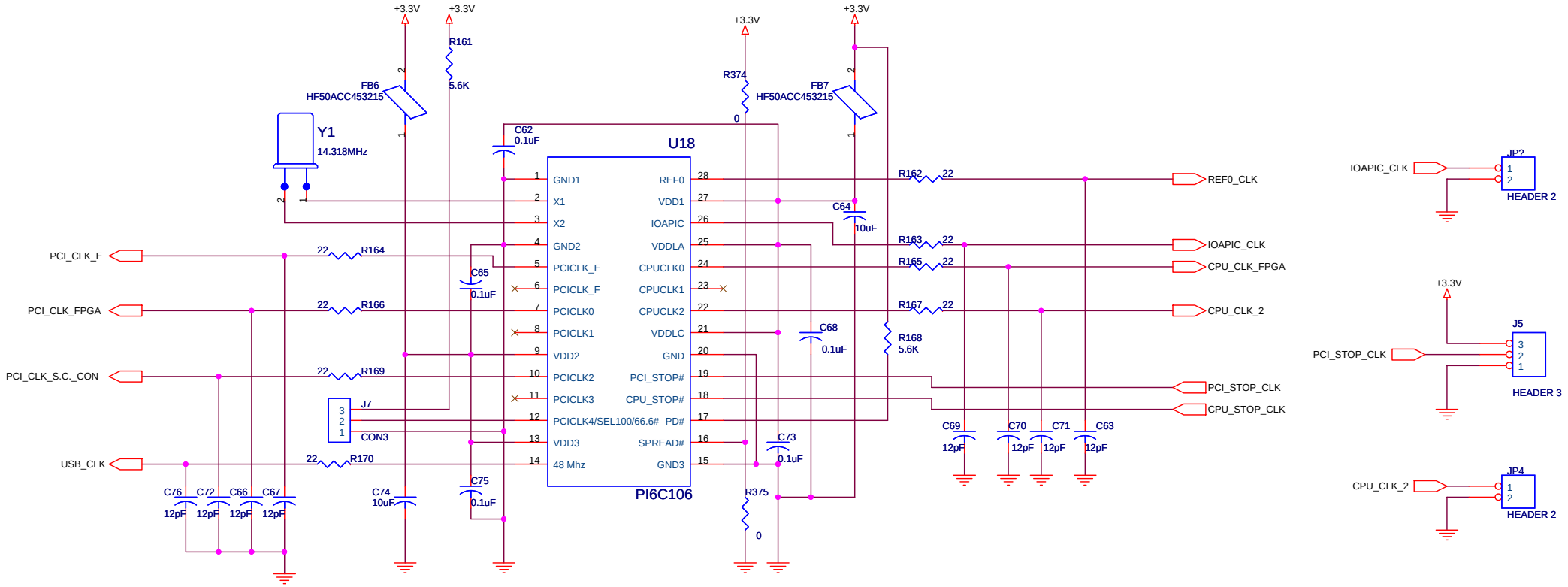

NOTES:

[1] BY SELECTING HIGH OR LOW INPUT THROUGH J7, 100 MHz OR 66.6 MHz CAN BE SELECTED RESPECTIVELY

[2] 12pF CAPACITORS ARE USED AS EMI REDUCING CAPACITORS

[3] STUFFING OPTIONS FOR SPREAD INPUT:
STUFFED R374 - DEFAULT HIGH
STUFFED R375 - ENABLE SPREAD#

MASTER CLOCK GENERATOR

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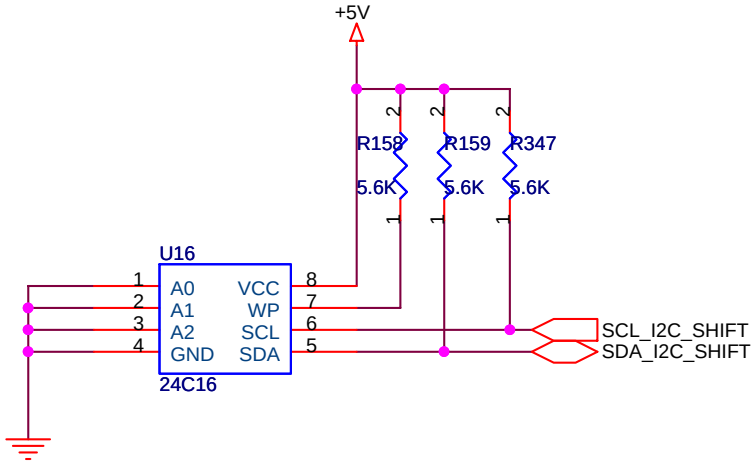

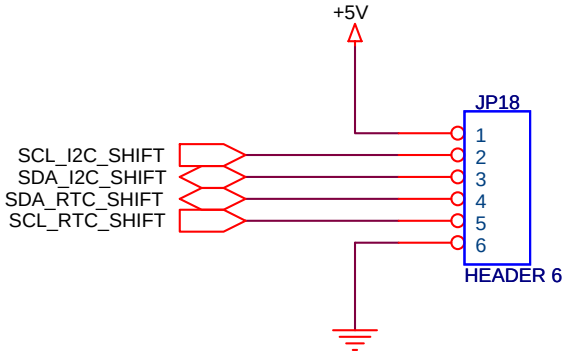

NOTES:

[1] R158 IS NOT STUFFED (WP PIN IS KEPT FLOATING) FOR NORMAL OPERATIONS
- STUFF R158 TO ENABLE WRITE PROTECTION IN THE SUPPORTED DEVICE
[2] FOR LEVEL SHIFTING, SEE PAGE_10_L.S. (FOR S.C.CONN.)

I2C PROM

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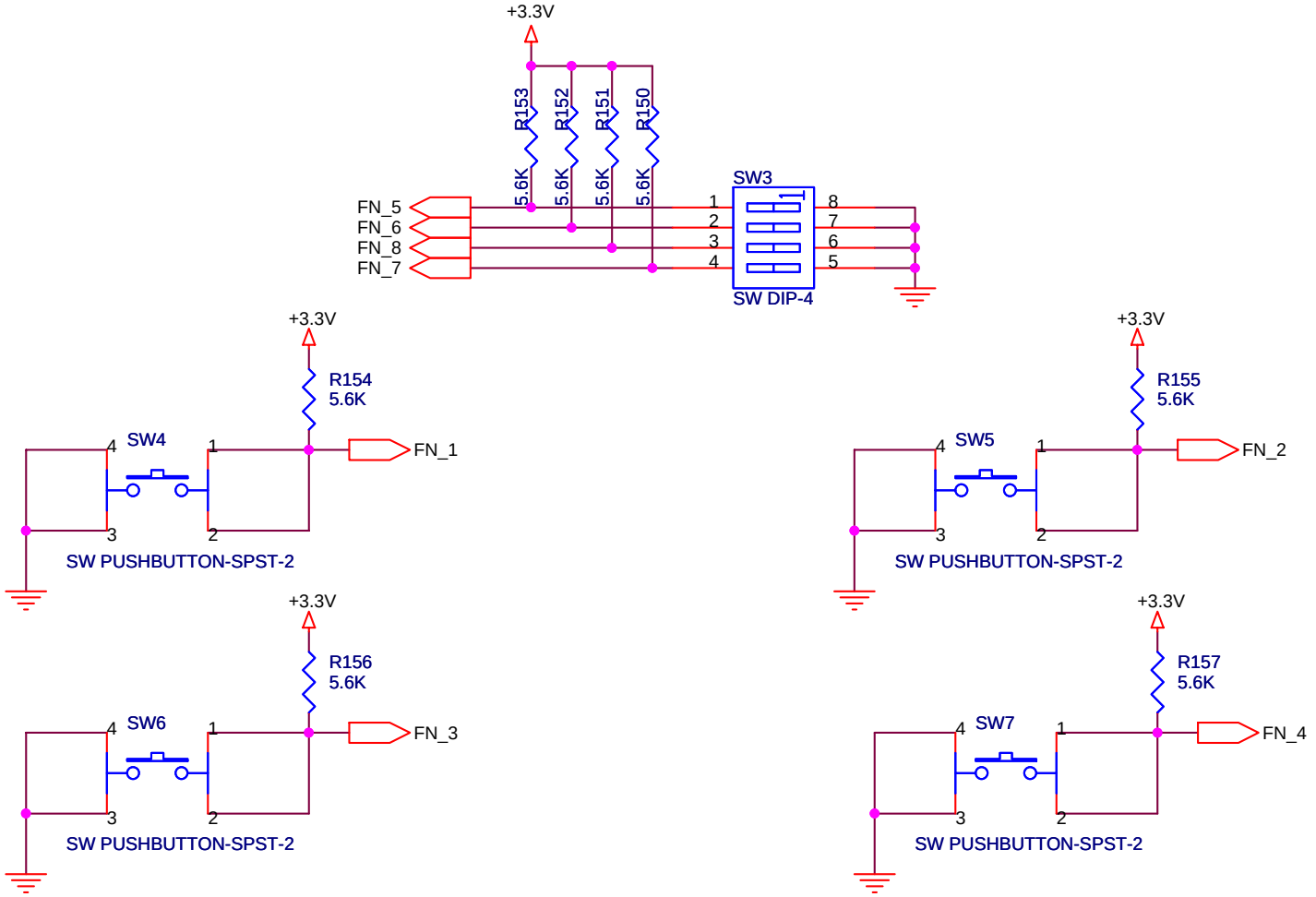

NOTES:

[1] HERE FOUR USER DEFINABLE PUSH BUTTON SWITCHES ARE SHOWN

[2] THE PUSH BUTTON SWITCH FOR SYSTEM RESET IS SEPARATELY DEFINED ON PAGE 16 (RESET CIRCUIT)

[3] BE CAREFUL WHEN MOUNTING THE DIP SWITCH

PUSH BUTTONS AND DIP SWITCHES

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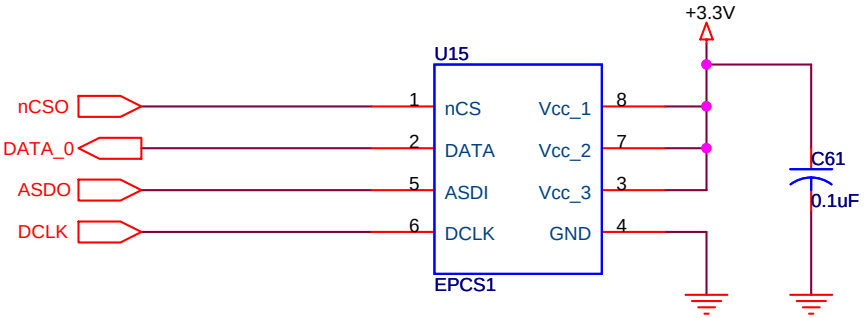
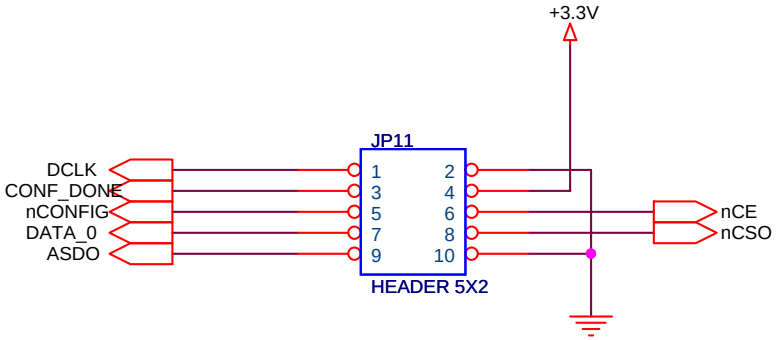
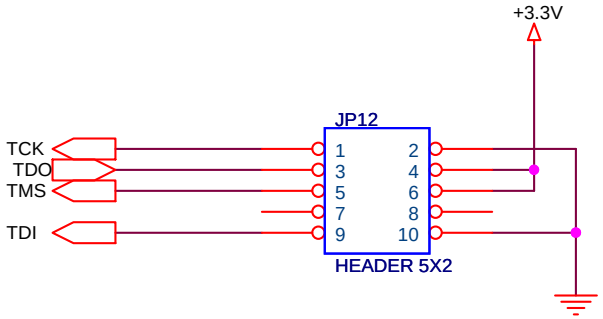




BYTE BLASTER II 10 PIN MALE HEADER FOR AS MODE [DCLK(FPGA) => DCLK(CONFIG. PROM)]



BYTE BLASTER II 10 PIN MALE HEADER FOR JTAG CONFIGURATION

CONFIGURATION PROM

Title: **UP3-1C6**		
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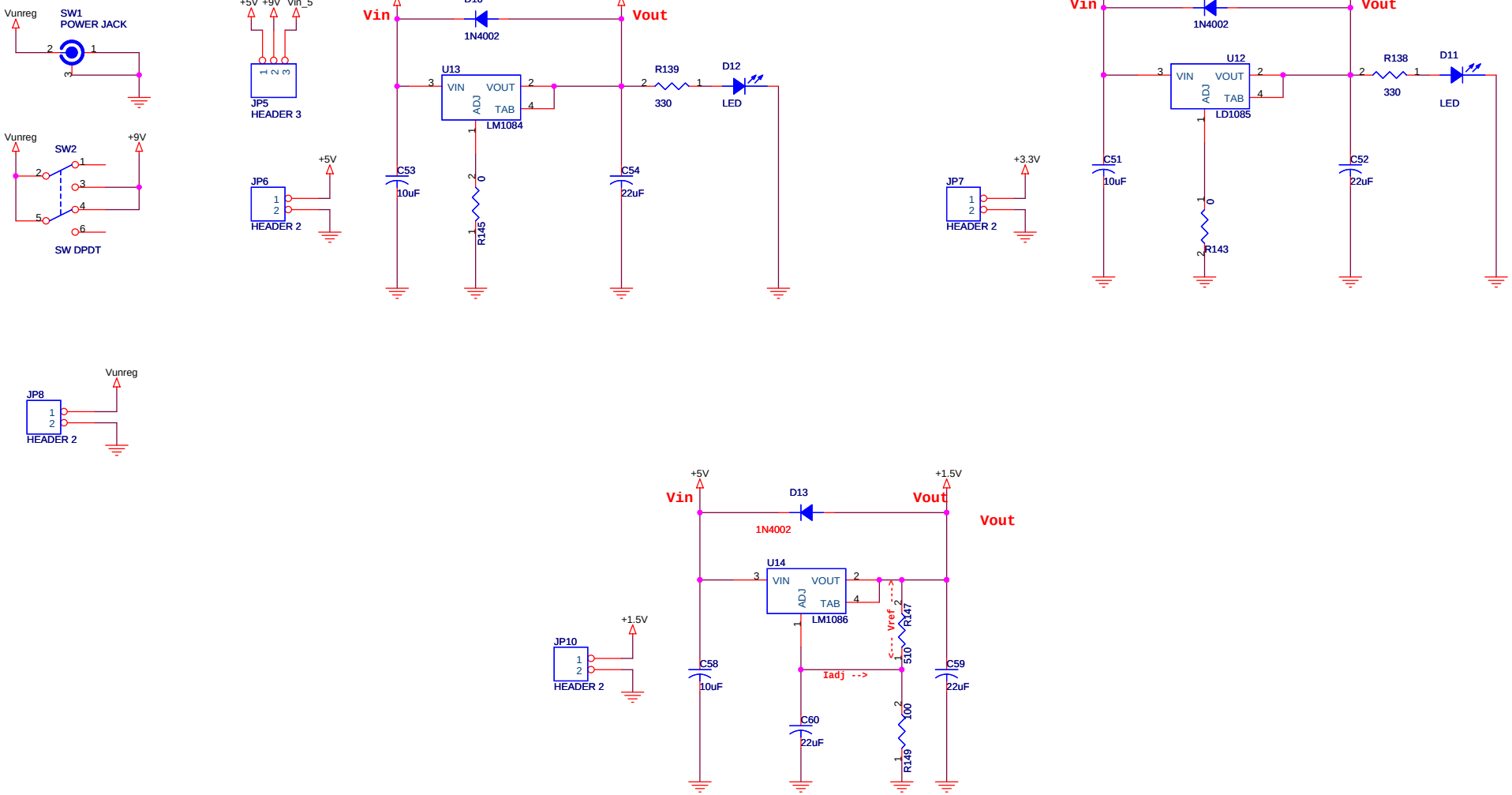

Vref = 1.25V
Iadj = 50uA

POWER SUPPLY CIRCUIT

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