Laboratory Exercise 7

This is an exercise in using finite state machines.

Part I

We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever $w = 1$ or $w = 0$ for four consecutive clock pulses the value of z has to be 1; otherwise, $z = 0$. Overlapping sequences are allowed, so that if $w = 1$ for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Use the toggle switch SW_0 on the Altera DE2 board as the input w, the LED $LEDG_0$ as the output z, and the pushbutton KEY_0 as the clock input which is applied manually.

1. Create a new project which will be used to implement the desired circuit on the Altera DE2 board.
2. Write a VHDL file that provides the necessary functionality.
3. Include the VHDL file in your project and compile the circuit.
4. Simulate the behavior of your circuit.
5. Assign the pins on the FPGA to connect to the switches and the LED, as indicated in the User Manual for the DE2 board.
6. Recompile the circuit and download it into the FPGA chip.
7. Test the functionality of your design by applying the input sequences and observing the output display.

Part II

We want to design a modulo-10 counter-like circuit that behaves as follows. It is reset to 0 by the *Reset* input. It has two inputs, w_1 and w_0, which control its counting operation. If $w_1w_0 = 00$, the count remains the same. If $w_1w_0 = 01$, the count is incremented by 1. If $w_1w_0 = 10$, the count is incremented by 2. If $w_1w_0 = 11$, the count is decremented by 1. All changes take place on the active edge of a *Clock* input. Use toggle switches SW_1 and SW_0 for inputs w_1 and w_0. Use the pushbutton KEY_0 as a manual clock. Display the decimal contents of the counter on the 7-segment display $HEX0$.

1. Create a new project which will be used to implement the circuit on the DE2 board.
2. Write a VHDL file that defines the circuit.
3. Include the VHDL file in your project and compile the circuit.
4. Simulate the behavior of your circuit.
5. Assign the pins on the FPGA to connect to the switches and the 7-segment display.
6. Recompile the circuit and download it into the FPGA chip.
7. Test the functionality of your design by applying some inputs and observing the output display.

Part III

In Exercise 4 you designed a circuit that displays the word HELLO in ticker tape fashion, on the eight 7-segment displays $HEX7-0$, such that the letters move from right to left in intervals of one second. Augment your design so that under the control of pushbuttons KEY_3 and KEY_2 the rate at which the letters move from right to left can be changed. If KEY_2 is pressed, the letters should move twice as fast. If KEY_3 is pressed, the rate has to be reduced by a factor of 2. Implement your circuit on the DE2 board and demonstrate that it works properly.