Laboratory Exercise 5

This is an exercise in implementing and using a real-time clock.

Part I

Implement a 3-digit BCD counter. Display the contents of the counter on the 7-segment displays, HEX2 - 0. Derive a control signal, from the 50-MHz clock signal provided on the Altera DE2 board, to increment the contents of the counter at one-second intervals. Use the pushbutton switch KEY_0 to reset the counter to 0.

- 1. Create a new project which will be used to implement the desired circuit on the DE2 board.
- 2. Write a Verilog file that specifies the desired circuit.
- 3. Include the Verilog file in your project and compile the circuit.
- 4. Simulate the designed circuit to verify its functionality.
- 5. Assign the pins on the FPGA to connect to the 7-segment displays and the pushbutton switch, as indicated in the User Manual for the DE2 board.
- 6. Recompile the circuit and download it into the FPGA chip.
- 7. Verify that your circuit works correctly by observing the display.

Part II

Design and implement a circuit that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7 - 6, the minute (from 0 to 60) on HEX5 - 4 and the second (from 0 to 60) on HEX3 - 2. Use the switches SW_{15-0} to preset the hour and minute parts of the time displayed by the clock.

Part III

Design and implement a reaction-timer circuit. The circuit is to operate as follows:

- 1. The circuit is reset by pressing the pushbutton switch KEY_0 .
- 2. After an ellapsed time of not less than four seconds, the LED labeled $LEDR_0$ turns on. At the same time a 3-digit BCD counter starts counting in intervals of one 1/100-th of a second.
- 3. A person whose reflexes are being tested must press the pushbutton KEY_3 as quickly as possible to turn the LED off and freeze the counter in its present state. The count which shows the reaction time will be displayed on the 7-segment displays $HEX_2 - 0$.

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