Using Large CPLDs and FPGAs for Prototyping and VGA Video Display Generation in Computer Architecture Design Laboratories

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Abstract

This paper describes current work utilizing a rapid prototyping approach to simulate, synthesize, and implement prototype digital system and computer architectures using PCs with student versions of commercial VHDL based CAD tools and a low cost board with a large CPLD or FPGA. VGA video output generated directly by the CPLD chip is used to display graphics or textual data eliminating the need for a logic analyzer. This low cost methodology is utilized in the design laboratory sequence of required courses for computer engineering students at Georgia Tech.

1. Introduction

New Computer Engineering students at Georgia Tech are now required to purchase their own PCs. Laboratories are still provided for students without PCs. This development, along with critical needs for instructional laboratory equipment, is providing an impetus to provide software and CAD tools for these student owned machines. PC based student versions of commercial digital logic CAD tools and higher gate capacity CPLD, Complex Programmable Logic Device, and FPGA, Field Programmable Gate Array, boards from Altera and Xilinx are now available. These developments have made it possible to provide students with logic synthesis and simulation CAD tools and to provide low cost hardware prototyping capability in the range of 20,000 to 70,000 logic gates.

Utilizing these new developments, laboratory assignments have been developed for the digital logic, computer architecture, and senior design classes at Georgia Tech.

Student versions of synthesis, simulation, and place and route tools are available from Altera and Xilinx. Low cost student or University CPLD and FPGA demo boards are available from both Altera and Xilinx. These boards could be checked out to students for use at home on a PC. The logic device is programmed via a PC parallel port connection.

Most of our laboratories were developed using the Altera student version tools and UP1 CPLD board, which were available several months earlier. Since the designs are written in VHDL they could be readily ported to other programmable logic CAD tools.

2. VGA Video from a CPLD or FPGA

In the past, the limited I/O features and debugging information available on CPLD and FPGA demo boards has been a problem on complex designs. To support this new laboratory development work, a VHDL based VGA video output feature was developed using hardware inside the CPLD or FPGA. Only five signals or pins are required, two sync signals and three RGB color signals. A simple resistor and diode circuit is used to convert TTL to the analog RGB signals. This circuit and a VGA connector is already installed on the Altera UP1 board [1].

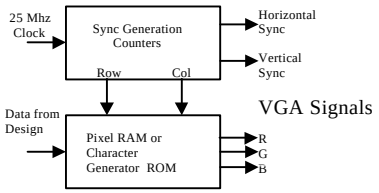

Figure 1: CPLD Generation of Video Signal. Only five external pins required for Video.

As seen in figure 1, a 25Mhz clock, which is the 640 by 480 VGA pixel data rate, is used to drive counters that generate the horizontal and vertical sync signals. Additional counters generate row and column addresses. The row and column addresses feed into a pixel RAM for

graphics data or a character generator ROM when used to display text. The required RAM or ROM is also synthesized inside the CPLD chip.

The pixel resolution was adjusted so that the video display hardware uses around one third of the logic gates on the 20,000 gate device. The VHDL video display code can be reused for different designs. This leaves ample room for all but the most ambitious student designs. By the turn of the century, CPLDs and FPGAs are forecast to have densities approaching 1,000,000 gates so much larger design options will soon be available.

3. Example Laboratory Assignments

Figure 2 shows a graphics mode video output generated directly by the CPLD board. It is running Conway's life game, a form of cellular automata. This was used as a state machine and memory laboratory assignment in the second digital logic class. Students were given the video hardware display module and had to develop the state machine to update generations in pixel memory using the rules for Conway's game of life.

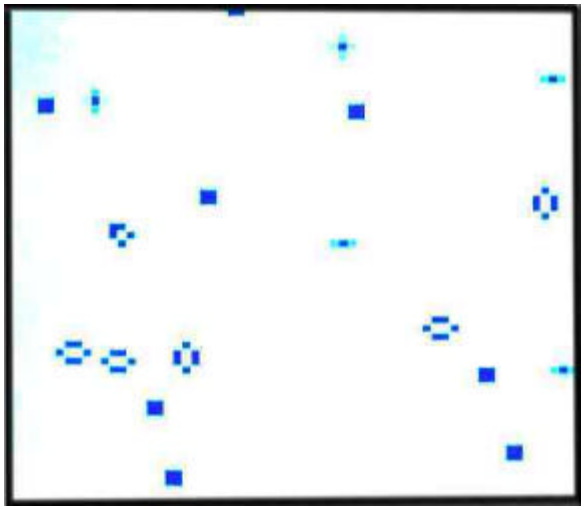

Figure 2: Graphics Mode VGA Output Generated by CPLD in Conway's Life Game.

In another digital logic lab, we reused this VGA graphics code and developed a train system animation and simulation. Students had to write a state machine to control the trains and switches to avoid collisions and implement a required travel path. Each quarter we can update the lab by changing the required path of the trains. The trains, tracks, sensors, and switches can be seen in figure 3.

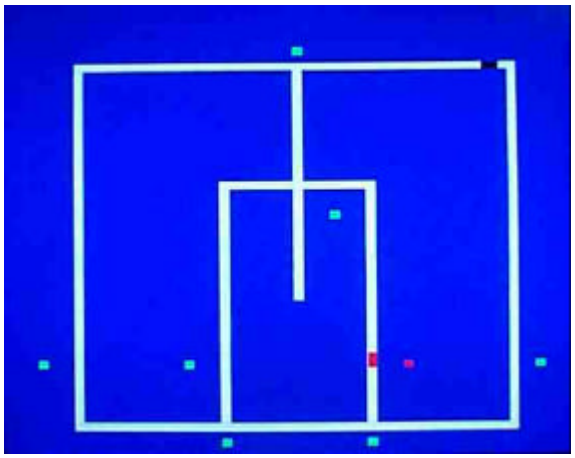

Figure 3: Video Output from Train Simulation in State Machine Laboratory Assignment.

For more complex designs, such as a computer, a few LEDs and switches do not provide enough information. In a laboratory environment, a logic analyzer would be used to capture additional data. These devices are expensive, take several minutes to attach and can require a significant number of normally scarce chip pins.

Since students would typically be working at home on these low cost boards, another approach was developed. A VHDL based logic analyzer feature was added to each design. The data from the logic analyzer was displayed by generating a VGA video signal directly in the FPGA. Students can attach their PC's VGA monitor to the FPGA board for use as a debugging tool.

Figure 4 shows the video output from a MIPS processor core developed for use in the computer architecture class. This design is VHDL based and it contains a character generator ROM with an 8 by 8 font for character display. Students were given the video display hardware module and logic analyzer code. Then they had to modify the MIPS model by adding new instructions and pipelining. The MIPS VHDL synthesis model was developed in an

earlier version of this course using another CAD tool and is described in more detail in [2].

In this laboratory, as in the others, simulation is used for debug prior to programming the CPLD device, since it provides a faster development cycle. A gate level timing simulation of the MIPS model run on the student version CAD tool is shown in Figure 5.

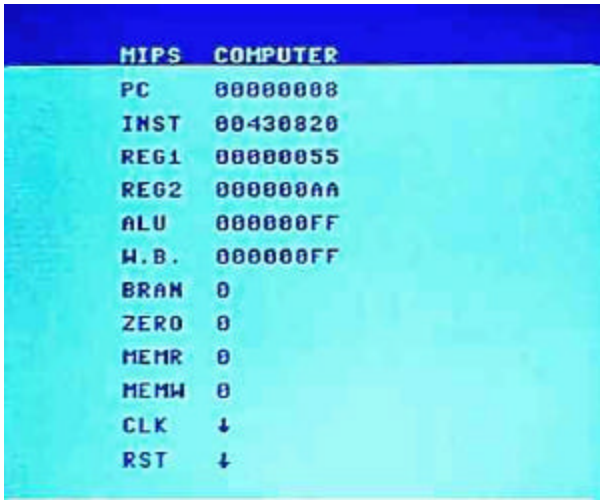

Figure 4: VGA Output from Internal CPLD Logic Analyzer in the MIPS Processor Model.

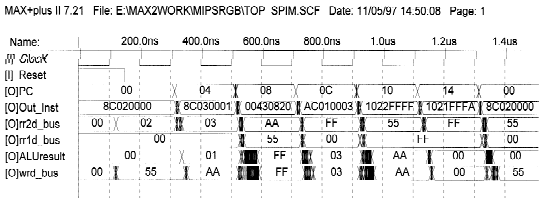

Figure 5: MIPS Processor Timing Simulation

The same approach of using the new CAD tools and CPLD boards was used to develop a new version of our computer engineering senior design laboratory. Previously this course used commercial workstation versions of CAD tools [3]. It also required significant CPU time on several Unix workstations. The availability of the workstations limited many of the designs.

Students in this course are already familiar with digital design, FPGAs, VHDL modeling, simulation, and synthesis, assembly language, C programming, and computer architecture from earlier required coursework. Students work together in teams of two to four on a six-month computer design project. Students are assigned the task of developing hardware and software for a pipelined RISC processor of their own design.

The rapid prototyping methodology used in the design process in this laboratory is shown in figure 5. VHDL synthesis [4] and a 70,000-gate FPGA/CPLD device are used to develop a working prototype. A meta assembler is configured by students to produce machine language test programs. Lcc, a retargetable C compiler [5] with a code generator generator, lburg, is used to develop a cross compiler for the student processor design. Object code is loaded into a ROM inside the CPLD. The Video display hardware modules and the logic analyzer code developed for the earlier computer architecture class were reused by students to monitor and debug their processor.

The Altera UP1 board contains a 20,000-gate CPLD chip, the FLEX 10K20. We carefully desoldered the 240 pin quad flat pack surface mount chip and replaced it with a pin compatible FLEX 10K70, which contains 70,000 gates. This allows us to work with larger designs in the senior design class and still use the low cost board.

One copy of the PC based commercial version of the CAD tools is checked out to each design since the student version is limited to 20,000 gates. Individual team members still use the student version to test smaller portions of the designs

After VHDL synthesis, the resulting schematic or netlist is then implemented on the CPLD device using commercial software, Altera's Max Plus II tools. Automatic generation of the data files to produce the prototype systems requires ten to thirty minutes of computer time for each large design. Designs can be downloaded to the FPGA/CPLD board in a few seconds. Prototype digital designs with up to 70,000 gates are possible with clock rates in the 10-25 megahertz range.

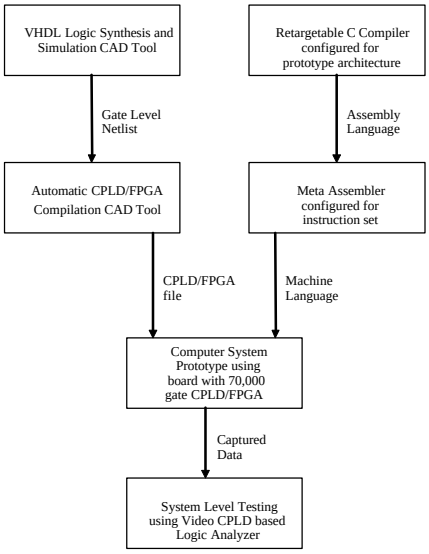

Figure 6: Rapid Prototyping Methodology

Last quarter, a five stage pipelined DLX processor was implemented by the students. The design required 42,000 gates and it successfully executed a bubble sort program on the CPLD board at a 12.5 MHz clock rate.

This quarter, students are working on adding a PS/2 keyboard input interface using the PS/2 connector on the Altera CPLD board, and a C compiler for their DLX processor implementation.

4. Conclusions

With the new PC based student version CAD tools on CDROMs and low cost CPLD and FPGA boards it is now possible for undergraduate students to design, simulate, and develop working prototypes of complex digital and computer systems as a routine part of their laboratory coursework using their own PCs. These tools can run very large problems on student PCs and the additional CPLD or FPGA boards required to implement a hardware design are comparable in price to a textbook. Source code files and documentation for all of the designs described in this paper are available from:

http://www.ece.gatech.edu/users/hamblen/ALTERA/altera.htm

5. Acknowledgments

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