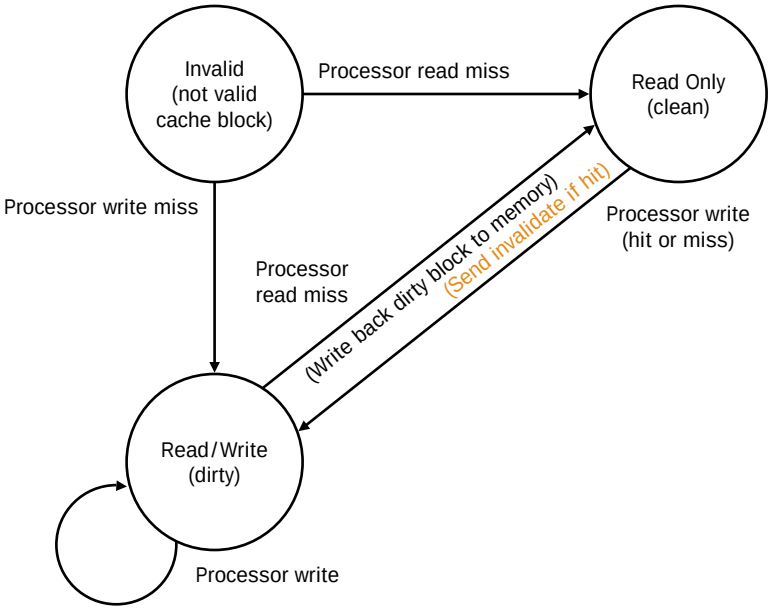
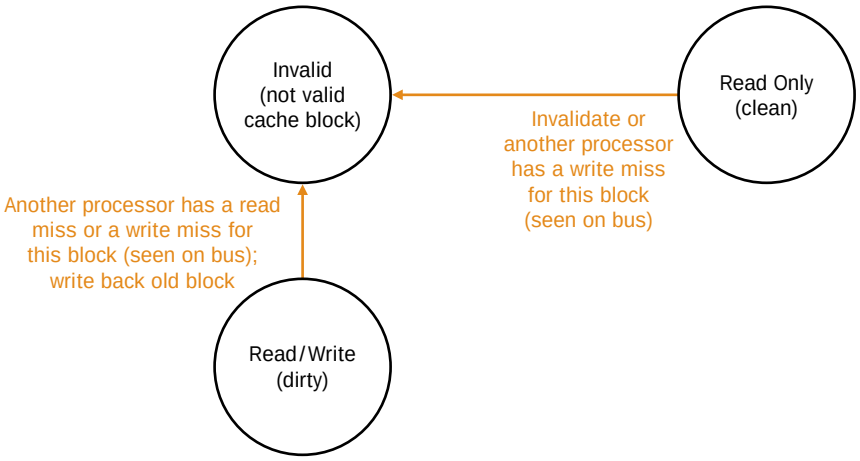


a. Cache state transitions using signals from the processor



b. Cache state transitions using signals from the bus