The ARM Architecture



The Architecture for the Digital World®

Agenda

Introduction to ARM Ltd

ARM Architecture/Programmers Model

Data Path and Pipelines

AMBA

Development Tools



ARM Ltd

- Founded in November 1990
- Spun out of Acorn Computers
- Designs a range of RISC processor cores
- Licenses ARM core designs to semiconductor partners who fabricate and sell to their customers.
 - ARM does not fabricate silicon itself
 - ARM is not the only company to design cores
- Develops technologies to assist with the design-in of the ARM architecture
 - Software tools, application software
 - Development boards, debug hardware
 - Bus architectures, peripherals, etc.



AR



ARM's Activities

4



ARM Connected Community – 550+



Silicon Partners

Treasure Actel 😤 DIE 🕢 altia 👫 elemenn 🖬 altia ang ang ang ang ang ang ang ang ang an
SanJisk 2 Control in the face and the face a
SHHIC STEPHIND OF FARADAY FLEXTRONICS KABEN
Auespec Synopsys: Synopsys: MNADEREED August A Synopsys: MNADEREED M
VeriSilicon Challan Con HUCONEX Acousti Open-Silicon Santonoucron
ZTEIC ZORAN QUALCOMM (C) RESERVED REAL REAL REAL REAL REAL REAL REAL REAL
Z ZTEIC ZORAN PRISO LINK QUALCOMM (C) STREAME AND REPORT IN
Silicon Challen (Purconex Concerts Concerts Concerts)
S SUNPLUS OF COLOSCOPIC MOMERTER DO SERVICES STORE

Design Support Partners Allum Amontec Marcian All Amontec Marcian Camerican Camerican SSEAN CARE BITRAN ARDITES AAI 🗢 EMThink Aff NSW CLASS (Conformer Fronting Consolutions Finder and Consolution Consolutions Conso REDACOM HCL TECHNOLOGIES HCL MC hitex HH Tech 公社会会会 HOYA LPC Tools" Same Decourse duolog = Qt. SEQUENCE Ortrinsity Sulistix sasken JASPER unnacue ant cip Silicon nonau Contraction Contracti Câdence Marajor States WIND RIVER Câdence Galance VOKOGAWA COULING Câdence United total Angela Câdence United total Angela Catological An Code_red Contect Conte REASTING SLITTERY'S ACTIVE ALLOSS REASTING C BITC 3. RASONANCE REGARDING Sophies and red ADMIECH PIS Coence DI TXTA Control Of SLOPE SOFTIAL

ARM

A moschip Sartonal

MXIC Manoradi

The ARM Business Model



Nokia N95 Multimedia Computer









OMAP[™] 2420 Applications Processor ARM1136[™] processor-based SoC, developed using Magma ® Blast® family and winner of

2005 INSIGHT Award for 'Most Innovative SoC'

Symbian OS[™] v9.2 Operating System supporting ARM processor-based mobile devices, developed using ARM® RealView® Compilation Tools

S60[™] 3rd Edition S60 Platform supporting ARM processor-based mobile devices

Mobiclip[™] Video Codec Software video codec for ARM processor-based mobile devices

ST WLAN Solution Ultra-low power 802.11b/g WLAN chip with ARM9[™] processor-based MAC

Connect. Collaborate. Create.





The Architecture for the Digital World®

Applications



The Architecture for the Digital World®





Agenda

Introduction to ARM Ltd

ARM Architecture/Programmers Model

Data Path and Pipelines

AMBA

Development Tools



Architecture Versions



Cortex family

Cortex-A8

- Architecture v7A
- MMU
- AXI
- VFP & NEON support

Cortex-R4

- Architecture v7R
- MPU (optional)
- AXI
- Dual Issue

Cortex-M3

- Architecture v7M
- MPU (optional)
- AHB Lite & APB







Relative Performance*



*Represents attainable speeds in 130, 90 or 65nm processes



Data Sizes and Instruction Sets

- The ARM is a 32-bit architecture.
- When used in relation to the ARM:
 - Byte means 8 bits
 - Halfword means 16 bits (two bytes)
 - Word means 32 bits (four bytes)
- Most ARM's implement two instruction sets
 - 32-bit ARM Instruction Set
 - 16-bit Thumb Instruction Set
- Jazelle cores can also execute Java bytecode





ARM and Thumb Performance



Thumb-2 Instruction Set



- Second generation of the Thumb architecture
 - Blended 16-bit and 32-bit instruction set
 - 25% faster than Thumb
 - 30% smaller than ARM
- Increases performance but maintains code density
- Maximizes cache and tightly coupled memory usage



EEMBC Analysis – Code Size

ARI



Processor Modes

- The ARM has seven basic operating modes:
 - User : unprivileged mode under which most tasks run
 - FIQ : entered when a high priority (fast) interrupt is raised
 - IRQ : entered when a low priority (normal) interrupt is raised
 - Supervisor : entered on reset and when a Software Interrupt instruction is executed
 - Abort : used to handle memory access violations
 - Undef : used to handle undefined instructions
 - System : privileged mode using the same registers as user mode



The ARM Register Set

Current Visible Registers



Exception Handling

When an exception occurs, the ARM:

- Copies CPSR into SPSR_<mode>
- Sets appropriate CPSR bits
 - Change to ARM state
 - Change to exception mode
 - Disable interrupts (if appropriate)
- 0x10 Stores the return address in LR_<mode> 0x0C
- Sets PC to vector address
- To return, exception handler needs to: 0x04
 - Restore CPSR from SPSR_<mode>
 - Restore PC from LR_<mode>

This can only be done in ARM state.

0x1C	FIQ
0x18	IRQ
0x14	(Reserved)
0x10	Data Abort
0x0C	Prefetch Abort
0x08	Software Interrupt
0x04	Undefined Instruction
0x00	Reset

Vector Table

Vector table can be at 0xFFFF0000 on ARM720T and on ARM9/10 family devices

Program Status Registers



- Condition code flags
 - N = Negative result from ALU
 - Z = Zero result from ALU
 - C = ALU operation Carried out
 - V = ALU operation oVerflowed
- Sticky Overflow flag Q flag
 - Architecture 5TE/J only
 - Indicates if saturation has occurred
- J bit
 - Architecture 5TEJ only
 - J = 1: Processor in Jazelle state

- Interrupt Disable bits.
 - I = 1: Disables the IRQ.
 - F = 1: Disables the FIQ.

T Bit

- Architecture xT only
- T = 0: Processor in ARM state
- T = 1: Processor in Thumb state
- Mode bits
 - Specify the processor mode

The Architecture for the Digital World®

Cortex-M3 Programmer's Model

Fully programmable in C

- Stack-based exception model
- Only two processor modes
 - Thread Mode for User tasks
 - Handler Mode for OS tasks and exceptions
- Vector table contains addresses





AR

Conditional Execution and Flags

- ARM instructions can be made to execute conditionally by postfixing them with the appropriate condition code field.
 - Increases code density
 - Improves performance by reducing the number of forward branch instructions.



 By default, data processing instructions do not affect the condition code flags but the flags can be optionally set by using "S". CMP does not need "S".







Branch instructions

- Branch: B{<cond>} label
- Branch with Link : BL{<cond>} subroutine_label



- The processor core shifts the offset field left by 2 positions, sign-extends it and adds it to the PC
 - ± 32 Mbyte range
 - How to perform longer branches?

AR

Classes of Instructions (v4T)



Data processing Instructions

- Consist of :
 - Arithmetic: ADD ADC SUB SBC RSB RSC
 - Logical: AND ORR EOR BIC
 - Comparisons: CMP CMN TST TEQ
 - Data movement: MOV MVN
- These instructions only work on registers, NOT memory.
- Syntax:

```
<Operation>{<cond>}{S} Rd, Rn, Operand2
```

- Comparisons set flags only they do not specify Rd
- Data movement does not specify Rn
- Second operand is sent to the ALU via barrel shifter.

Using a Barrel Shifter: The 2nd Operand



Register, optionally with shift operation

- Shift value can be either be:
 - 5 bit unsigned integer
 - Specified in bottom byte of another register.
- Used for multiplication by constant

Immediate value

- 8 bit number, with a range of 0-255. Rotated right through even number of positions
- Allows increased range of 32-bit constants to be loaded directly into registers

Single register data transfer

LDR	STR	Word
LDRB	STRB	Byte
LDRH	STRH	Halfword
LDRSB		Signed byte load
LDRSH		Signed halfword load

Memory system must support all access sizes

Syntax:

- LDR{<cond>}{<size>} Rd, <address>
- STR{<cond>}{<size>} Rd, <address>

e.g. LDREQB

AR

Agenda

Introduction to ARM Ltd ARM Architecture/Programmers Model

Data Path and Pipelines

AMBA

Development Tools



The ARM7TDM Core



ARM9E-S Datapath



Pipeline changes for ARM9TDMI

ARM7TDMI





ARM10 vs. ARM11 Pipelines

ARM10



					Shift	ALU	Saturate	
	Fetch 1	Fetch 2	Decode	Issue	MAC 1	MAC 2	MAC 3	Write back
-					Address	Data Cache 1	Data Cache 2	



Full Cortex-A8 Pipeline Diagram





Agenda

Introduction to ARM Ltd ARM Architecture/Programmers Model Data Path and Pipelines AMBA

Development Tools



An Example AMBA System



AHB Structure



ARM®

Agenda

Introduction to ARM Ltd ARM Architecture/Programmers Model Data Path and Pipelines AMBA

Development Tools



ARM Debug Architecture



The Architecture for the Digital World®

Keil Development Tools for ARM



- Includes ARM macro assembler, compilers (ARM RealView C/C++ Compiler, Keil CARM Compiler, or GNU compiler), ARM linker, Keil uVision Debugger and Keil uVision IDE
- Keil uVision Debugger accurately simulates on-chip peripherals (I²C, CAN, UART, SPI, Interrupts, I/O Ports, A/D and D/A converters, PWM, etc.)
- Evaluation Limitations
 - 32K byte object code + 32K data limitation
 - Some linker restrictions such as base addresses for code/constants
 - GNU tools provided are not restricted in any way
- http://www.keil.com/demo/



Keil Development Tools for ARM

🕎 Hello - µVision3 - [C:\Keil\ARM\Exa	imples\Hello\Hello.c]	
Eile Edit View Project Debug Flash	n Pe <u>r</u> ipherals <u>T</u> ools <u>S</u> VCS <u>W</u> indow <u>H</u> elp	_ B ×
· [찹 🝃 🖬 🗿 👗 🖻 🛍 오 오 淳 ·	╪ѧ%%%% %	
👔 \$0 10 40 40 40 40 40 40 40 40 40 40 40 40 40	Q Ø ♥ ¥ ■ E 器 G >	
🔮 🕮 🖀 🕌 🛱 🔊 LPC2100		
Project Workspace		
Register Value	02 /* This file is part of the uVision/ARM development tools */	_
Current	03 /* Copyright KEIL ELEKTRONIK GmbH 2002-2004 */	
R0 0x000000c	04 /************************************	
R1 0x000000c	U5 /* */*	
R2 UXUUUUUU2U	00 /* millo.c. herro worrd Example */	
B4 0x0000000	08 //***********************************	
R5 0x0000000	09	
R6 0x00000000	10 #include <stdio.h> /* prototype declarations for I/O functions */</stdio.h>	
R7 0x0000000	11 #include <lpc21xx.h> /* LPC21xx definitions */</lpc21xx.h>	
R8 0x00000000	12	
R9 0x00000000 ▼	14 /***********/	
	15 /* main program */	
	16 /**************/	
Symbols	17 int main (void) { /* execution starts here */	
Mask: X		
	13 /* initialize the serial interface */ DINGELO = 0Y000500000. /f Enable PyD1 and TyD1 */	
Name Type 🔺	21 ULCR = 0x83; /* 8 bits, no Parity, 1 Stop bit */	
E VI Simulator VTREG	22 U1DLL = 97; /* 9600 Baud Rate @ 15MHz VPB Clock */	
Peripheral SFR	23 U1LCR = 0x03; /* DLAB = 0 */	
ALDOM uchai	24	
ALDOY ushort	<pre>25 printf ("Hello World\n"); /* the 'printf' function call */</pre>	
ALHOUR uchar	2b while (1) ((t in embedded program does not stop and t/	-
→	A Bindenined brobraw lides not stop and "	
→	🖹 Hello.c 🖹 Startup.s 🚉 Disassembly <i></i> Serial #2	
* MISSING DEVICE (ROD3. SECUR	ITY KEY NOT FOIND)	
 Running in Eval Mode 	Address, Ux4000	
Load "C:\\Keil\\ARM\\Example	es\Hello\\Obj\\Hello.ELF"	00
-		00
*** Restricted Version with	16384 Byte Code Size Limi 0x0000401A: 00 00 00 00 00 00 00 00 00 00 00 00 00	
*** Currently used: 1980 By		
Nop -		
		00
ASSIGN BreakDisable BreakEn	able BreakKill BreakList 🔽 👔 👔 🛛 🖉 🛛 🕞 🕫 🖉	
	► B M ► ► ► ► Memory #1 (Memory #2) Memory #3) Memory #4 /	
Ready	Simulation t1: 0.72642057 sec L:29 C:1	

TI's Beagle Board



he Digital World®





Questions: university@arm.com

More information: www.arm.com/community/university



The Architecture for the Digital World®

