

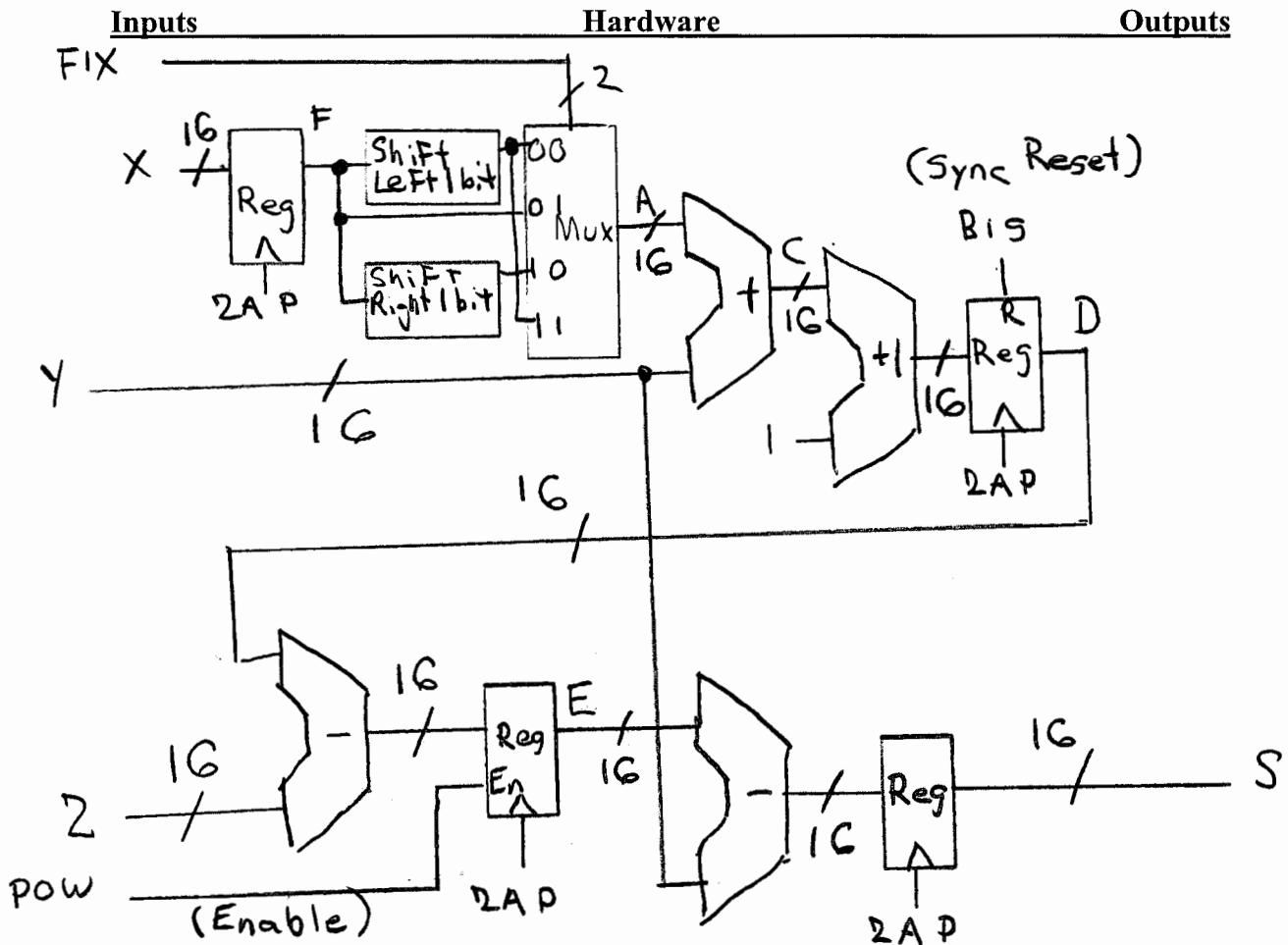
Score: _____

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ECE 3055 Quiz Wednesday, March 30, 2011

In the space below, draw a block diagram of the hardware synthesized by the VHDL code found on the additional page provided with the quiz. In the block diagram, include the following:

1. Show all input signals on the left and outputs on the right.
2. Draw each hardware unit in a style similar to the textbook's block diagrams.
3. Include and clearly indicate any registers, clock signals, enables, and resets.
4. Label all signals with their VHDL signal name (both internal and external).
5. Use a "/" with a number to indicate the width of any busses (more than 1-bit).
6. Number each of the mux's input signals with it's corresponding decimal number (i.e. the value on the mux's control input signal that selects each input).
7. Indicate # of bits and direction for any shifts and indicate if resets are sync or async.



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LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY test IS
    PORT( X, Y, Z      : IN STD_LOGIC_VECTOR( 15 DOWNT0 0 );
          BIG, ZAP, POW : IN STD_LOGIC;
          FIX          : IN STD_LOGIC_VECTOR(1 DOWNT0 0);
          S            : OUT STD_LOGIC_VECTOR( 15 DOWNT0 0 ));
END test;

ARCHITECTURE behavior OF test IS
    SIGNAL A, B, C, D, E, F : STD_LOGIC_VECTOR( 15 DOWNT0 0 );

BEGIN
    A <= F WHEN FIX(1 DOWNT0 0) = "01" ELSE '0' & F(15 DOWNT0 1)
        WHEN FIX(1 DOWNT0 0) = "10" ELSE F(14 DOWNT0 0) & '0';
    C <= A + Y;

    PROCESS
    BEGIN
        WAIT UNTIL ZAP'EVENT AND ZAP = '1';
        IF BIG = '1' THEN D <= X"0000";
        ELSE
            D <= C + 1;
        END IF;
        IF POW = '1' THEN E <= D - Z;
        END IF;
        F <= X;
        S <= E - Y;
    END PROCESS;

END behavior;

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