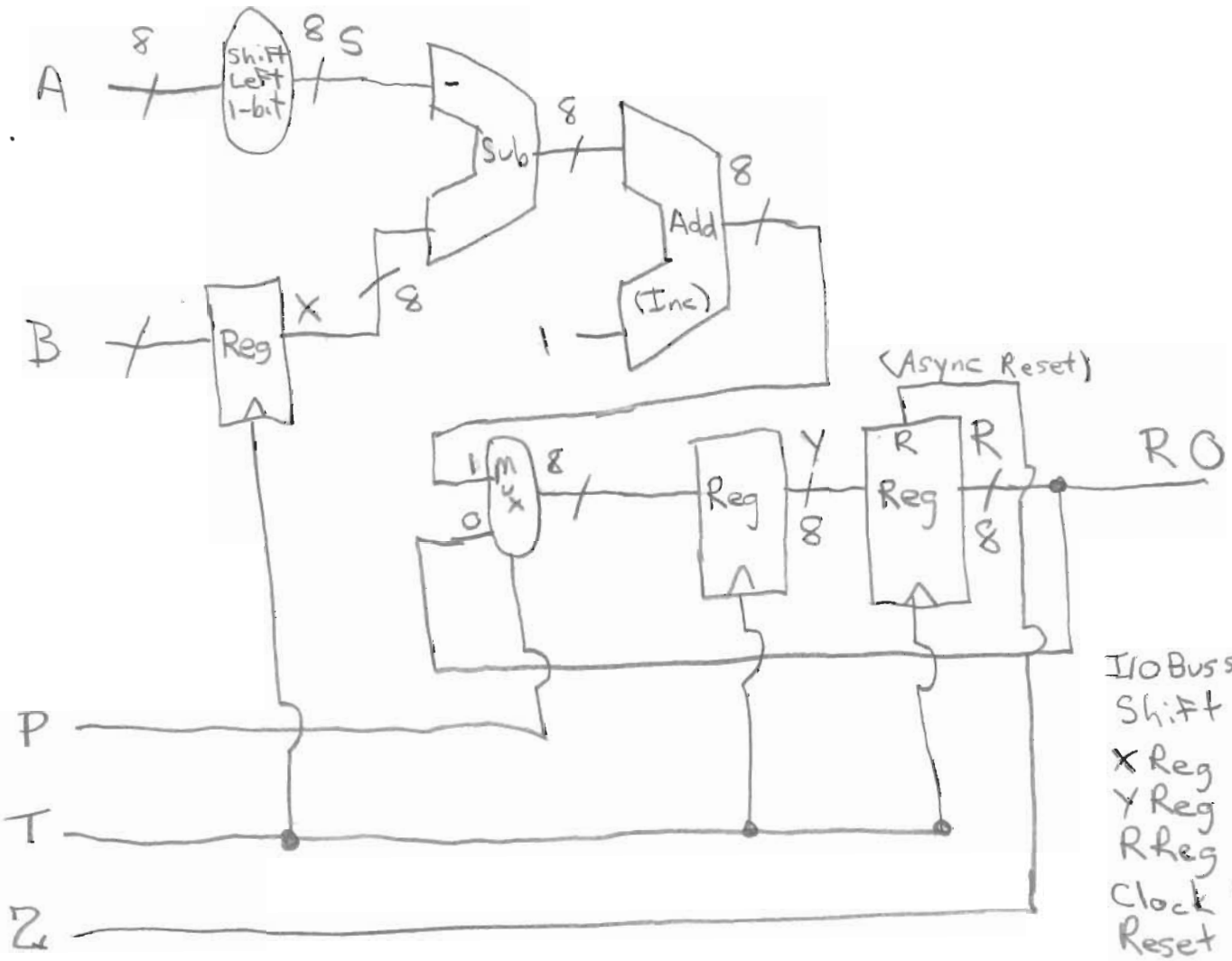
Score: _____ Name: _____

ECE 3055 Quiz 9 Wednesday, October 27

In the space below, draw a block diagram of the hardware synthesized by the VHDL code found on the additional page provided with the quiz. In the block diagram, include the following:

1. Show all input signals on the left and outputs on the right.
2. Draw each hardware unit in a style similar to the textbook's block diagrams.
3. Include and clearly indicate any registers, clock signals, and resets.
4. Label all signals with their VHDL signal name (both internal and external).
5. Use a "/" with a number to indicate the width of any busses (more than 1-bit).
6. Number each of the mux's input signals with it's corresponding decimal number (i.e. the value on the mux's control input signal that selects each input).
7. Indicate # of bits and direction for any shifts and indicate if resets are sync or async.

Inputs **Hardware** **Outputs**



I/O Bus 5+2e
Shift
X Reg
Y Reg
R Reg
Clock
Reset
Mux
Add
Sub
1pt each

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;
ENTITY  test9 IS
        PORT( A, B    : IN     STD_LOGIC_VECTOR( 7 DOWNTO 0 );
                P, T, Z  : IN    STD_LOGIC;
                RO       : OUT  STD_LOGIC_VECTOR( 7 DOWNTO 0 ));
END test9;
ARCHITECTURE behavior OF test9 IS
SIGNAL X, Y, S, C, R : STD_LOGIC_VECTOR( 7 DOWNTO 0 );
BEGIN
 RO <= R;
 S <= A(6 DOWNTO 0) & "0";
 C <= (X - S) + 1;
 PROCESS (Z,T)
        BEGIN
         IF Z='1' THEN R<=X"00";
         ELSIF (T'EVENT AND T='1') THEN
                R <= Y;
                X <= B;
                IF P='1' THEN Y <= C; ELSE Y <= R;
                END IF;
        END IF;
 END PROCESS;
END behavior;
```