Score:_____ Name:_____

ECE 3055 Quiz - March 24, 2004

1. What is the average time to read or write a sector on a disk drive that has an average seek time of 10 ms. The drive rotates at 7,200 RPM, has a transfer rate of 40 megabytes per second, and 2048 byte sectors. Assume the disk is idle and there is a .05 ms controller overhead per sector. (*Note*: In I/O device transfer rates, MB is always 10^6 bytes – not 2^{20} bytes!)

3 pts. $10ms + \frac{.5}{(7200/60)} + \frac{2048}{40\times10^6} + 0.05 = 10 + 4.16 + .0512 + .05$

Average R/W time per sector = 14.27 **(in ms.)**

2. In problem 1, assume the disk has an internal cache. When a (sector) read hit occurs the cache transfers the data at the same speed to the controller as a normal disk sector read operation (assuming the head is instantly over the correct sector) and the same controller overhead applies. How much faster could the read sector operation time be with a cache hit? (compute the maximum increase and assume maximum seek time is twice the average)

2 pts. $20ms + \frac{1}{(7200/60)} + \frac{2048}{40\times10^6} + 0.05 = 28.43$ vs. $\frac{2048}{40\times10^6} + 0.05 = .1012$

A Disk Cache read sector hit is up to 281 **times faster.**

3. The PCI express bus about to appear in new PCs is a 1-bit serial bus with up to a 10Ghz clock. It contains all of the signals used in the older parallel PCI bus. PCI express uses shift registers to convert them to 1-bit serial over a high-speed wire and then back to parallel at the other end of the wire. Assuming that 25% of the clock cycles are used to send address and other bus control signals (leaving 75% for data) what is the maximum data transfer rate that can be achieved using one PCI express wire?

2 pts. $10 \times .75 \times 10^9/8$

Maximum I/O bandwidth = 937 **(in megabytes per second)**

4. Briefly summarize the characteristics of asynchronous vs. synchronous busses, and then compare and contrast their advantages and disadvantages.

3 pts.

synchronous
- common clock
- need limited length and loading
- Faster bus not much logic

asynchronous
- no common clock
- uses handshake lines
- automatically adjusts for longer busses and more loading
- somewhat slower & more logic