Score:_____ Name:_____

ECE 3055 Quiz - March 15, 2011

Assume a 256-line 2 way set associative TLB (i.e, 512 total data entries) is used in a system with 36-bit virtual byte addresses, 32-bit physical memory byte addresses, and 64K byte pages. For the sequence of virtual addresses shown below in hex, state whether each address causes a TLB hit or miss and show the physical address generated. The TLB is initially empty after power on and the set on the left gets the first entry in each line. A LRU replacement policy is used. A portion of the page table entries and TLB are listed below. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Virtual Address	*Hit/Miss*	*Physical Address*
000003E2	M	F200 03E2
00003E3	H	F200 1E3
100030012	M	D000 0012
000000171	M	F000 0171
200300E1	M	0ACE 00E1
100030153	H	D000 0153

TLB Final Contents

Line:	*Set #1 Valid*	*Tag*	*Data*	*Set #2 Valid*	*Tag*	*Data*
0	1	000	F000			
1						
2						
3	1	200 / 000	0ACE / F200	1	100	0000

Page Table Initial Contents

Virtual Page #	*Data*
00000	F000
00001	3000
00002	B000
00003	F200
...	...
00030	FFFF
00031	D0D0
...	...
10000	B200
10003	D000
10000	E000
10030	6500
10031	6000
20003	0ACE