Score:_____ Name:_____

ECE 3055 Quiz - March 17, 2010

Assume a 16-line 2 way set associative TLB (i.e, 32 total data entries) is used in a system with 36-bit virtual byte addresses, 32-bit physical memory byte addresses, and 4K byte pages. For the sequence of virtual addresses shown below in hex, state whether each address causes a TLB hit or miss and show the physical address generated. The TLB is initially empty after power on and the set on the left gets the first entry in each line. A LRU replacement policy is used. A portion of the page table entries are listed below. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Virtual Address	*Hit/Miss*	*Physical Address*
000000171	M	920001 71
0000300E1	M	D0000GE1
000010153	M	B2000153
0000303E2	H	D0003E2
0000311E3	M	E0001E3
000000012	M	92000012

TLB Final Contents

Line:	*Set #1 Valid*	*Tag*	*Data*	*Set #2 Valid*	*Tag*	*Data*
0	1	00000	92000	1	00003	D0000
1	1	00003	E0000	0	X	X
2	0	X	X	0	X	X
3	0	X	X	0	X	X

Page Table Initial Contents

Virtual Page #	*Data*
000000	92000
000001	30000
000002	F0000
000003	E2000
…	…
000010	B2000
…	…
000030	D0000
000031	E0000
000032	65000
000033	60000