Score:_____ Name:_____

ECE 3055 Quiz 8 - October 22, 2004

Assume a 256-entry direct-mapped TLB is used in a system with a 36-bit virtual byte addresses, 32-bit physical memory byte addresses, and 64K byte pages. For the sequence of virtual addresses shown below in hex, state whether each address causes a TLB hit or miss and show the physical address generated. The TLB is initially empty after a power on reset. Assume all listed page table entries are valid. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Address	*Hit/Miss*	*Physical Address*
000000171	M	E0000171
000022CE2	M	5F002CE2
000022AE3	H	5F002AE3
000002031	H	E0002031
000003055	H	E0003055
000020153	H	5F000153

TLB Initial Contents (Empty)

Block	*Valid*	*Tag*	*Data*
0	0	X	X
1	0	X	X
2	0	X	X
3	0	X	X

TLB Final Contents

Block	*Valid*	*Tag*	*Data*
0	1	000	E000
1	0	X	X
2	1	000	5F00
3	0	X	X

Page Table Initial Contents

Virtual Page #	*Data*
00000	E000
00001	F000
00002	5F00
00003	3000
…	
00020	7200
00021	2000
00022	F000
00023	D200