Score:_____ Section:_____Name:_____

ECE 3055 Quiz 7 – Wednesday March 9 , 2011

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 1M entries, 16-bit data, and ties into a 32-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

Cache before

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	0	X	X
4	0	X	X
5	1	0	FFFF

Cache after

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	1	11	CABE
4	1	5	0ACE
5	1	4	5555

Memory before

Address	*Data*
00110003	4321
00040003	FACE
00040005	5555
00050004	0BAA

Memory after

Address	*Data*
00100002	CABE
00040002	FACE
00040005	5555
00050004	CACE

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*
00000005	Read		Y
00400005	Read		N
00500004	Read		N
00400003	Read		N
00400003	Read		Y
01100003	Read		N
00400003	Read		N
00500004	Write	0ACE	
00400005	Read		Y
01100003	Write	CABE	

Cache miss rate (include reads only) = 62.5 %