Score:_____ Name:_____

ECE 3055 Quiz 7 - October 22, 2010

Assume a 16-entry direct-mapped TLB is used in a system with 36-bit virtual byte addresses, 32-bit physical memory byte addresses, and 4K byte pages. For the sequence of virtual addresses shown below in hex, state whether each address causes a TLB hit or miss and show the physical address generated. The TLB is initially empty after power on and the initial contents of the page table are given. Assume all listed page table entries are valid. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Address (TLB | Page)	*TLB Hit/Miss*	*Physical Memory Address*
000001012	M	30000012
0000000E1	M	920000E1
000030153	M	D0000153
000000171	M	92000171
0000303E2	M	D00003E2
000033 1E3	M	60001E3

2 pts. 2 pts.

TLB Initial Contents

Block	*Valid*	*Tag*	*Data*
0	0	X ~~0~~ 0	X
1	0	~~X~~ 3 0	X
2	0	X	X
3	0	~~X~~ 3	X

TLB Final Contents

Block	*Valid*	*Tag*	*Data*
0	1	00003	D0000
1	1	00000	30000
2	X	X	X
3	1	00003	60000

6 pts.

Page Table Initial Contents

Virtual Page #	*Data*
000000	92000
000001	30000
000002	F0000
000003	E2000
…	…
000030	D0000
000031	E0000
000032	65000
000033	60000