Score:_____ Section:_____ Name:_____

# ECE 3055 Quiz 7 – Wednesday March 10, 2010

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 256 entries, 32-bit data, and ties into a 32-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

**Cache before**

| *Block* | *Valid* | *Tag* | *Data* |
|---|---|---|---|
| 1 | 0 | X | X |
| 2 | 0 | X | X |
| 3 | 0 | ~~X~~ 400 1000 | X 400 |
| 4 | 0 | ~~X~~ 500 | X |
| 5 | 0 | ~~X~~ 401 | X |

**Cache after**

| *Block* | *Valid* | *Tag* | *Data* |
|---|---|---|---|
| 1 | 0 | X | X |
| 2 | 0 | X | X |
| 3 | 1 | 400 | C0EE0000 |
| 4 | 1 | 500 | 0ECE0000 |
| 5 | 1 | 401 | 789A 0000 |

**Memory before**

| *Address* | *Data* |
|---|---|
| 00100003 | 0000ACE |
| 00040003 | 12340000 |
| 00040105 | 789A0000 |
| 00050004 | 00000ABE |

**Memory after**

| *Address* | *Data* |
|---|---|
| 00100003 | C0000ACE |
| 00040003 | 00EE0000 |
| 00040105 | 789A0000 |
| 00050004 | 0ECE0000 |

**Memory requests**

| *Address* | *Type* | *Data* | *Hit(y/n)* |
|---|---|---|---|
| 00050004 | Read | | n |
| 00040003 | Read | | n |
| 00040105 | Read | | n |
| 00100003 | Read | | n |
| 00040003 | Read | | n |
| 00050004 | Write | 0ECE0000 | |
| 00040105 | Read | | Y |
| 00040003 | Write | 00EE0000 | |
| 00050004 | Read | | Y |
| 00040003 | Read | | Y |

256 = $2^8$

Cache hit rate (include reads only) = 37.5 %