Score:_____ Section:_____ Name:_____

ECE 3055 Quiz - October 14, 2009

1. A two-way set associative cache is given the memory operations shown below. It contains four lines and has one word per block. A LRU (Least Recently Used) replacement policy is used on this cache. The cache is initially empty. The first column of the cache gets the first entry after the valid bits have been reset. In the blanks provided in the Cache below, fill in the final address values only (i.e., a 12 in a blank, means address and data for memory location 12 is in cache) and compute the miss rate. Address values are shown in decimal.

Memory Read Operations

Address	Hit (Y/N)?
2	N
4	N
8	N
5	N
21	N
17	N
19	N
64	N
2	Y
6	N
9	N
8	Y
43	N
917	N

12/14

Final Cache Contents

Block	Element 1	Element 2
0	4 64	8 9
1	8 17 917	21
2	2	6
3	19	43

Miss rate for all memory operations is 85.7 (%)

2. A cache takes 1 clock cycle for a hit and an additional 20 clock cycles for a miss. If the hit rate is 95% compute the AMAT in clock cycles.

$1 + .05 \times 20 = 2$

AMAT = 2