Score:_____ Name:_____

ECE 3055 Quiz 7 - October 15, 2008

A four-way set associative cache is given the memory operations shown below. It contains four lines and has one word per block. A LRU (Least Recently Used) replacement policy is used on this cache. The cache is initially empty except for the two entries shown. The first column of the cache gets the first entry after the valid bits have been reset and then it fills left to right. In the blanks provided in the Cache below, list the original address value only (i.e. 12 in blank, means tag address and data for memory location 12 is in cache). Address values are shown in decimal.

Memory Read Operations

Address	Hit (Y/N)?
4	Y
1	Y
5	N
19	N
25	N
8	N
4	Y
21	N
22	N
1	Y
13	N
22	Y
23	N
5	N
999	N
401	N

Final Cache Contents

Block	Element 1	Element 2	Element 3	Element 4
0	4	8		
1	1	813	~~25~~ 5	~~21~~ 401
2	22			
3	19	23	999	

Hit rate for all memory operations is 31.25 (%)