Score:_____ Name:_____

ECE 3055 Quiz 7 - March 3, 2009

Assume a 256-entry direct-mapped TLB is used in a system with a 40-bit virtual byte addresses, 32-bit physical memory byte addresses, and 64K byte pages. For the sequence of virtual addresses shown below in hex, state whether each address causes a TLB hit or miss and show the physical address generated. The TLB is initially empty after a power on reset. Assume all listed page table entries are valid. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Virtual Address	*Hit/Miss*	*Physical Address*
000000017F	M	E000 017F
0000022CE2	M	F0F0 2CE2
0000022AE3	H	F0F0 2AE3
000000203F	H	E000 203F
0000003055	H	E000 3055
0000020153	H	F0F0 0153

TLB Initial Contents (Empty)

Block	*Valid*	*Tag*	*Data*
0	0	X	X
1	0	X	X
2	0	X	X
3	0	X	X

TLB Final Contents

Block	*Valid*	*Tag*	*Data*
0	1	0000	E000
1	0	X	X
2	1	0000	F0F0
3	0	X	X

Page Table Initial Contents

Virtual Page #	*Data*
000000	E000
000001	F000
000002	F0F0
000003	3000
…	
000020	7200
000021	2000
000022	F000
000023	D200