Score:_____ Section:_____ Name:_____

ECE 3055 Quiz 7 - October 8, 2003

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 4096 entries, 16-bit data, and ties into a 24-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

Cache before

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	0	X	X
4	0	X	X
5	0	X	X

Cache after

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	1	100	000F
4	1	040	0ABE
5	1	040	6789

2 pts.

Memory before

Address	*Data*
100003	FACE
040003	1234
040004	0ABE
040005	6789

Memory after

Address	*Data*
100003	000F
040003	1234
040004	0ABE
040005	6789

1

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*
040003	Read		M
040004	Read		M
040005	Read		M
100003	Write	000F	
040025	Read		H
040003	Read		M
040004	Read		H
040005	Read		H
100003	Read		M

2

Cache miss rate (include reads only) = 62.5 %

1

$4096 = 2^{12}$

3 hex digits to address Cache memory