

Score: _____

Name: _____

ECE 3055 Quiz 6 - July 1, 2002

A four-way set associative cache is given the memory operations shown below. It contains two lines and has one word per block. A LRU (Least Recently Used) replacement policy is used on this cache. The cache is initially empty except for the two entries shown. The first column of the cache gets the first entry after the valid bits have been reset and then it fills left to right. In the blanks provided in the Cache below, list the original address value only (i.e. 12 in blank, means address and data for memory location 12 is in cache).

Memory Read Operations

Address Hit (Y/N)?

0 N

Final Cache Contents

1 N

Block **Element 1** **Element 2** **Element 3** **Element 4**

5 N

0 ~~20~~ ~~4~~ 6 14

9 N

1 ~~25~~ 13 ~~21~~ ~~5~~

25 N

6 N

1 Y

14 N

20 N

4 N

20 Y

4/6

21 N

21 Y

Hit rate for all memory operations is 25 (%)

5 N

6 Y

3 N