Score:_____ Section:_____ Name:_____

ECE 3055 Quiz 6 – Wednesday October 13 , 2010

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 64K entries, 16-bit data, and ties into a 32-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

Cache before

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	~~X~~ 4 → 04	X
3	0	X	X
4	0	~~X~~ 5	X
5	0	~~X~~ 4	X

Cache after

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	1	0004	FACE
3	0	X	X
4	1	0005	0ECE
5	1	0004	0ABE

Memory before

Address	*Data*
00100002	1234
00040002	0ACE
00040005	0ABE
00050004	0BAA

Memory after

Address	*Data*
00100002	1234
00040002	FACE
00040005	0ABE
00050004	0ECE

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*
00040002	Read		N
00100002	Read		N
00040005	Read		N
00040002	Read		N
00050004	Write	0ECE	
00040005	Read		Y
00040002	Write	FACE	
00040005	Read		Y
00050004	Read		Y
00040002	Read		Y

64K

Cache miss rate (include reads only) = 50 %