Score:_____ Section:_____ Name:_____

ECE 3055 Quiz 6 – Wednesday October 6, 2004

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 4K entries, 16-bit data, and ties into a 32-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

Cache before

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	0	X	X
4	0	X	X
5	0	X	X

Cache after

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	1	00100	00EE
4	1	00050	0ECE
5	1	00040	789A

6 pts.

Memory before

Address	*Data*
00100003	0ACE
00040003	1234
00040005	789A
00050004	0ABE

Memory after

Address	*Data*
00100003	00EE
00040003	1234
00040005	789A
00050004	0ECE

2 pts.

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*
00040003	Read		N
00050004	Write	0ECE	
00040005	Read		N
00100003	Write	00EE	
00040005	Read		Y
00040005	Read		Y
00050004	Read		Y
00040003	Read		N
00040005	Read		Y
00100003	Read		N

tag

1 pt.

Cache miss rate (include reads only) = 50 %

1 pt.