Score:_____ Section:_____ Name:_____

ECE 3055 Quiz 5 - October 9, 2002

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 65,536 entries, 16-bit data, and ties into a 24-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Immediately after powering up, the cache is initially empty and all valid bits are reset to indicate entries are invalid. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex. "X" means undefined.

Cache before

Block	*Valid*	*Tag*	*Data*
1	0	X	X
2	0	X	X
3	0	X	X
4	0	X	X
5	0	X	X

Cache after

Block	*Valid*	*Tag*	*Data*	
1	1	10	0001	(2)
2	1	04	6789	(2)
3	1	04	0ABE	(2)
4	0	X	X	~
5	0	X	X	~

Memory before

Address	*Data*
100001	FACE
040001	1234
040002	6789
040003	0ABE

Memory after

Address	*Data*	
100001	0001	(1)
040001	1234	~
040002	6789	~
040003	0ABE	~

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*	
040001	Read		n	(1)
040002	Read		n	
040003	Read		n	
100001	Write	0001		
040001	Read		n	(2)
040002	Read		y	
040003	Read		y	
100001	Read		n	

One wrong (-1)

Two or more wrong (-2)

Cache hit rate (include reads only) = 28.6 % (1)

Miss Rate instead of Hit Rate (-1)

Full Credit for hit Rate if CORRECT based on WRONG answers