

Score: _____

Name: _____

ECE 3055 Quiz V, Wednesday, October 2

The program below is executed on the 5 stage pipelined MIPS described in chapter 6. Answer the following questions about this program.

```

loop:  lw    $4,100($0)
       lw    $3,300($4)
       lw    $7,200($0)
       slt   $8,$7,$3
       beq   $8,$4,then
       and   $6,$7,$8
       addi  $5,$5,6
then:  or    $8,$5,$8
       sw    $5,100($6)
       beq   $5,$0,loop

```

Assume the control unit **does not have** any hazard detection, forwarding, a new branch compare circuit, or automatic branch flushing, and that the register file will not write and then read a new register value in one clock cycle. Rewrite the code sequence by adding the minimum number of NOP instructions (do not reorder or change instructions) to eliminate all potential data and branch hazards. Assume other non-NOP instructions follow the last branch in the original code sequence above.

Total number of NOPs required 18

← 4 pts.
-1 each nop off ±

```

lw      addi
nop     nop
nop     nop
nop     nop
lw      or
lw      sw
nop     beq
nop     nop
nop     nop
slt     nop
nop     nop
nop     nop
nop     nop
beq     nop
nop     nop
nop     nop
and

```

Assume the control unit is improved by adding the hazard and forwarding unit as outlined in the text and the current lab assignment, adding a branch compare unit to the decode stage, and the register file writes then reads a new value in a single clock cycle. Determine the number of clock cycles required to complete the first loop execution (i.e. executes code in loop and branches back to top of loop and is just ready to fetch sw again) of the original code sequence. Assume the inner branch is not taken.

For 13 (no fill)
-2

Assume the processor starts this program initially at power up. if there were no hazards or branch

flushing, the original program would require 14 clock cycles for execution. (include the time to initially fill the pipeline).

← 3 pts.

But this program will need to stall and/or flushes the pipeline an additional 3 clock cycles so

a total of 17 clock cycles is required for execution (include the time to initially fill the pipeline).

← 3 pts.
-1 each clock cycle off