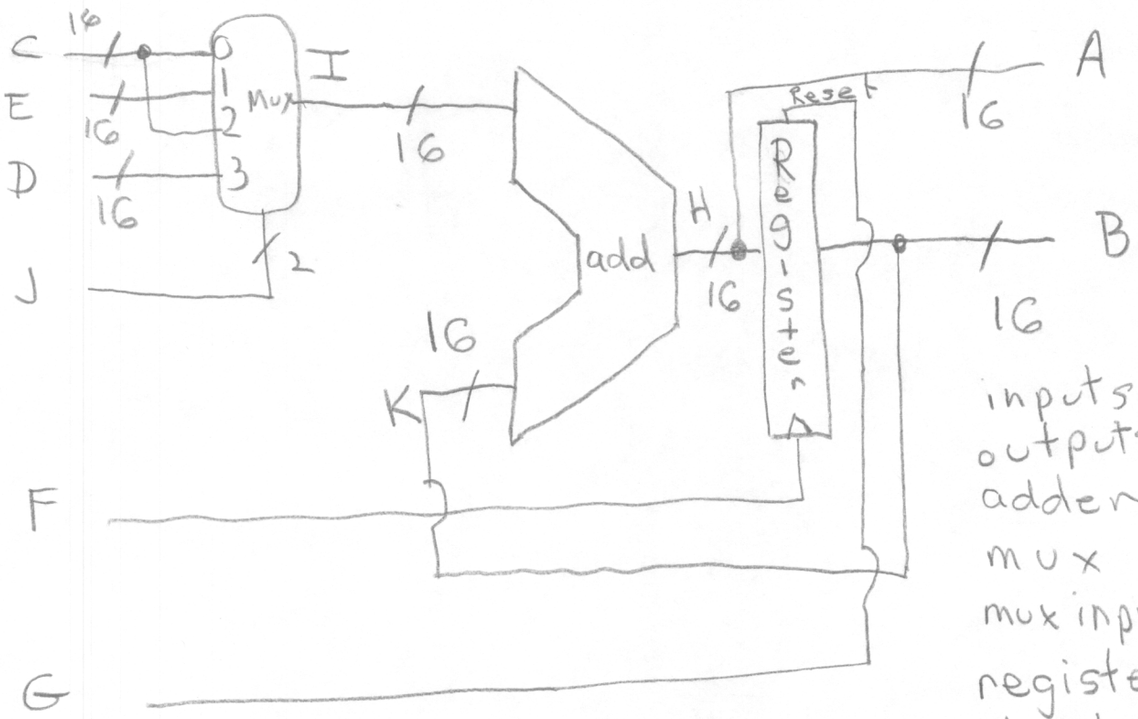
Score: _____ Name: _____

ECE 3055 Quiz IV, Wednesday, September 25

Part I: (*9 pts.*) In the space below, draw a block diagram of the hardware synthesized by the VHDL code found on the additional page provided with the quiz. In the block diagram, include the following:

1. Show all input signals on the left and outputs on the right.
2. Draw each hardware unit in a style similar to the textbook's block diagrams.
3. Include and clearly indicate any registers, clock signals, and resets.
4. Label all signals with their VHDL signal name (both internal and external).
5. Use a "/" with a number to indicate the width of any busses (more than 1-bit).
6. Number each of the mux's input signals with it's corresponding decimal number (i.e. the value on the mux's control input signal that selects each input).

Inputs **Hardware** **Outputs**



	pts.
inputs	1
outputs	1
adder	1
mux	1
mux inputs	1
register	2
clock	1
reset	1

Part II: (*1pt.*) Why is internal signal K needed in VHDL? (Explain)

You can not read an out signal (B) in VHDL so an internal signal is needed. The internal signal is copied to the out signal.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;
ENTITY test IS
    PORT(   SIGNAL A, B      : OUT   STD_LOGIC_VECTOR( 15 DOWNTO 0 );
            SIGNAL C, D, E   : IN    STD_LOGIC_VECTOR( 15 DOWNTO 0 );
            SIGNAL F, G      : IN    STD_LOGIC;
            SIGNAL J         : IN    STD_LOGIC_VECTOR(1 DOWNTO 0));
END test;
ARCHITECTURE behavior OF test IS
    SIGNAL H, I, K       : STD_LOGIC_VECTOR( 15 DOWNTO 0 );
BEGIN
        A <= H;
        B <= K;
        I  <=   C WHEN J(0) = '0'
                ELSE D WHEN J(1) = '1'
                ELSE E;
        H  <= I + K;
    PROCESS
        BEGIN
            WAIT UNTIL ( F'EVENT ) AND ( F = '1' );
            IF G = '1' THEN
                  K <= "0000000000000000" ;
            ELSE
                  K <= H;
            END IF;
    END PROCESS;
END behavior;
```