Score:_____ Section:_____Name:_____

ECE 3055 Quiz 5 - June 26, 2002

A direct mapping cache with WTWA (i.e. Write Through Write Allocate) is used to reduce the average memory access time on a computer. This cache holds 4096 entries, 16 bit data, and ties into a twenty-bit address bus with no byte or word select bits. Determine the contents of the cache and memory below after the memory requests shown are sent to the cache. Keep track of hits and misses so you can compute the cache miss rate when you are done. All values are in hex.

Cache before

Block	*Tag*	*Data*
1	~~20~~ 40	~~FFFF~~ 0ACE
2	50	CABE
3	~~2~~ 50	~~0ACE~~ 0000
4	~~20~~ 40	~~FACE~~ BABA ~~BABA~~ CABE
5	5	0001

Cache after

Block	*Tag*	*Data*
1	40	0ACE
2	50	CABE
3	50	0000
4	20	BABA
5	05	0001

Memory before

Address	*Data*
20004	BABA
50003	~~FACE~~ 0000
40001	~~1234~~ 0ACE
40004	CABE

Memory after

Address	*Data*
20004	BABA
50003	0000
40001	0ACE
40004	CABE

Memory requests

Address	*Type*	*Data*	*Hit(y/n)*
20004	Read		Y
40001	Write	0ACE	
50003	Write	0000	
50003	Read		Y
40004	Read		N
40001	Read		Y
20004	Read		N

Cache miss rate (include reads only) = 40 %