Score: _____ Name: _____

ECE 3055 Quiz III Wednesday, February 17, 2010

The following sequence of MIPS instructions is clocked into the basic unimproved pipeline (i.e., no forwarding, hazard, or branch flush units) shown in Figure 4.51 on page 362 of your textbook. Examine this figure carefully to see exactly where each signal is located (i.e. before or after pipeline registers). At the end of Clock cycle 5, when all instructions are in the pipeline, indicate the resulting values **in hexadecimal** in the spaces provided below. Assume all data memory locations contain the word address of the location, and that the address in any LW/SW instructions below is already shown as a word address (not byte!). Assume that each register contains a value equal to the register number prior to execution of this code. List the *actual value* produced by the hardware design described in the text – even if the value is not used or saved.

sub	**$6, $5, $6**	WB
lw	**$9, 4($7)**	DM
add	**$12, $12, $15**	EX
and	**$3, $4, $7**	ID
or	**$4, $2, $17**	IF

Instruction = 0x 00871824 *(2 pts)*

Read Data 1 = 0x 00000004 *(1 pt)*

Read Data 2 = 0x 00000007 *(1 pt)*

ALU Result = 0x 0000001B *(1 pt)*

(Data Memory) Address = 0x 0000000B *(1 pt)*

Write Data (input at register file after mux) = 0x FFFFFFFF *(1 pt)*

Write Register (Address) = 0x 06 *(1 pt)*

ALU control (4 or 3-bits in binary) = 0010 *(1 pt)*

ALUSrc = 0 *(1/2 pt)*

MemRead = 1 *(1/2 pt)*