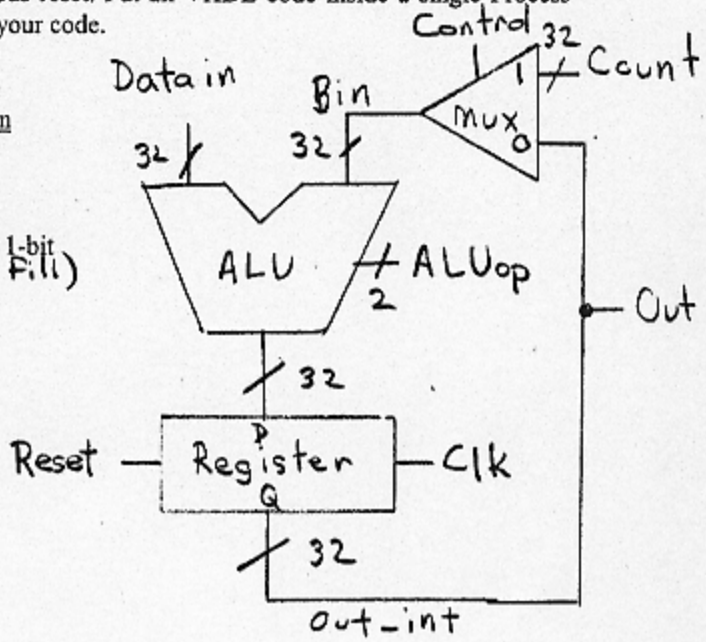
5. *(20 points)* Write a complete VHDL synthesis model for the digital hardware shown in the block diagram. Use a positive edge clock with a synchronous reset. Put all VHDL code inside a single Process block. The signal, Bin may or may not be required in your code.

ALUop	Operation
00	add
01	subtract
02	OR
03	Shift left 1-bit (zero Fill)



library 2
entity 2
arch
bin mux 2
out 2
Process
ALU Case 3
ALU Ops 3
Register 3
Reset 3
Extra registers -2 each
Not in Process -5

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;
ENTITY  test1c IS
 PORT( Datain,Count          : IN  STD_LOGIC_VECTOR( 31 DOWNTO 0 );
       ALU_Op                : IN  STD_LOGIC_VECTOR( 1 DOWNTO 0 );
       Control,clk,reset     : IN  STD_LOGIC;
       OUT                   : OUT STD_LOGIC_VECTOR( 31 DOWNTO 0 ));
END test1c;
ARCHITECTURE behavior OF test1c IS
SIGNAL  Bin, OUT_int   : STD_LOGIC_VECTOR( 31 DOWNTO 0 );
BEGIN
 Bin <= OUT_int WHEN Control='0' ELSE Count;
 OUT <= OUT_int;
PROCESS
 BEGIN
  WAIT UNTIL clk'EVENT AND clk='1';
   IF reset='1' THEN Outp_int <= "00000000000000000000000000000000";
   ELSE
     CASE ALU_op IS
       WHEN "00"  => Out_int <= Datain + Bin;
       WHEN "01"  => Out_int <= Datain - Bin;
       WHEN "10"  => Out_int <= Datain OR Bin;
       WHEN "11"  => Out_int <= Datain(30 Downto 0) & "0";
       WHEN OTHERS => Out_int <= "00000000000000000000000000000000";
      END CASE;
   END IF;
 END PROCESS;
END behavior;
```