

Score: \_\_\_\_\_

Name: \_\_\_\_\_

### ECE 3055 Quiz III, Wednesday, February 4, 2004

The following sequence of MIPS instructions is clocked into the pipeline shown on page 472-476 of your textbook. Examine this figure carefully to see exactly where each signal is located (i.e. before or after pipeline registers). At the end of Clock cycle 5, Indicate the resulting register values in **hexadecimal** in the spaces provided below. Assume all data memory locations contain the word address of the location, and that the address in any LW/SW instructions below is already shown as a word address (not byte!). Assume that each register contains a value equal to the register number prior to execution of this code. List the actual value produced by the hardware design described in the text – even if the value is not used or saved.

sw	\$7, 8	wb
sw	\$2, 0x345(\$1)	dm
add	\$3, \$7, \$3	ex
or	\$2, \$5, \$6	dec
lw	\$7, 30	Fetch

Instruction = 0x 00A61025 (2 pts)

Read Data 1 = 0x 00000005 (1 pt)

Read Data 2 = 0x 00000006 (1 pt)

ALU Result = 0x 0000000A (1 pt)

(Data Memory) Address = 0x 346 (1 pt)

Write Data (input at register file after mux) = 0x 00000007 (1 pt)

Write Register (Address) = 0x 07 (1 pt)

ALU control (3-bits in binary) = 010 (1 pt)

ALU op (2-bits) = 10 (1/2 pt)

RegWrite = 0 (1/2 pt)