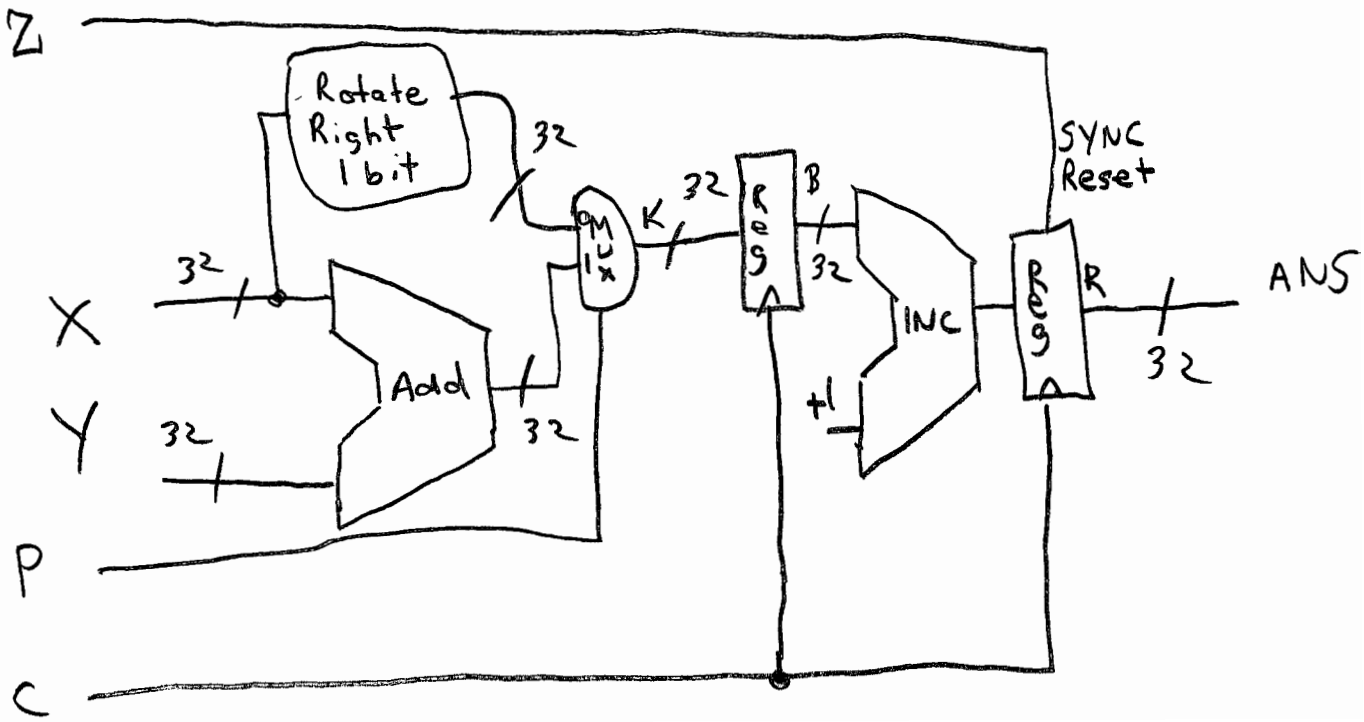
Score: _____ Name: _____

ECE 3055 Quiz Wednesday, November 5

In the space below, draw a block diagram of the hardware synthesized by the VHDL code found on the additional page provided with the quiz. In the block diagram, include the following:

1. Show all input signals on the left and outputs on the right.
2. Draw each hardware unit in a style similar to the textbook's block diagrams.
3. Include and clearly indicate any registers, clock signals, and resets.
4. Label all signals with their VHDL signal name (both internal and external).
5. Use a "/" with a number to indicate the width of any busses (more than 1-bit).
6. Number each of the mux's input signals with it's corresponding decimal number (i.e. the value on the mux's control input signal that selects each input).
7. Indicate # of bits and direction for any shifts and indicate if resets are sync or async.

Inputs **Hardware** **Outputs**



```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_ARITH.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;

ENTITY  test10 IS
        PORT(X, Y    : IN     STD_LOGIC_VECTOR( 31 DOWNTO 0 );
                    P, C, Z  : IN          STD_LOGIC;
                    ANS          : OUT  STD_LOGIC_VECTOR( 31 DOWNTO 0 ));
END test10;

ARCHITECTURE behavior OF test10 IS

SIGNAL  A, B, S, K, R : STD_LOGIC_VECTOR( 31 DOWNTO 0 );

BEGIN
  ANS <= R;
  S <= X(0) & X(31 DOWNTO 1);
  K <= Y + X WHEN P = '1' ELSE S;
  PROCESS
         BEGIN
          WAIT UNTIL C'EVENT AND C='1';
          IF Z='1' THEN R <= X"00000000";
          ELSE
             R <= B + 1;
          END IF;
          B <= K;
  END PROCESS;
END behavior;
```