Score:_____ Name:_____

The following RISC assembly language program is executed on a MIPS processor. Fill in the register values that will be present, after execution of this program. A summary of MIPS instructions is included at the bottom of the page – for anyone unfamiliar with the MIPS instruction set. Prior to execution of the program, memory location 0x0200 contains 0x30552030. Note: 0x indicates hexadecimal and all answers must be in hexadecimal. A MIPS memory word or register contains 32-bits.

```
        LW      $5, 0x0200
        ADD     $3, $5, $5
        OR      $4, $5, $3
        SRL     $2, $4, 8
        XOR     $6, $5, $2
        SUB     $6, $5, $3
        BNE     $5, $2, LABEL1
        SUB     $6, $0, $2
LABEL1: SW      $6, 0x0200
```

After execution of the MIPS code sequence above,

R2 = 0x 0070FF60 (*in hexadecimal*)

R3 = 0x 60AA4060 (*in hexadecimal*)

R4 = 0x 70FF6070 (*in hexadecimal*)

R5 = 0x 30552030 (*in hexadecimal*)

2 pts./blank

-1 off 1 hex digit

Memory Location 0x0200 contains: 0x CFAADFDO (*in hexadecimal*)

The MIPS processor contains thirty-two 32-bit registers, $0 through $31. $0 always contains a zero. By default, all arithmetic operations use two's complement arithmetic.

MIPS Instruction			***Meaning***
ADD	Rd, Rs, Rt	-	Rd = Rs + Rt (R – register ($))
OR	Rd, Rs, Rt	-	Rd = Rs bitwise logical OR Rt
BNE	Rs, Rt, *address*	-	Branch to *address*, only if Rs not equal to Rt
LW	Rd, *address*	-	LOAD - Rd gets contents of memory at *address*
SRL	Rd, Rs, *count*	-	Shift right logical (*use 0 fill*) by *count* bits
SUB	Rd, Rs, Rt	-	Rd = Rs - Rt
SW	Rd, *address*	-	STORE - memory at *address* gets contents of Rd
XOR	Rd, Rs, Rt	-	Rd = Rs bitwise logical XOR Rt