Score:_____ Name:_____

ECE 3055 Test II

1. *(5%)* A virtual memory system has 32-bit virtual addresses (*byte addressable* 32-bit words) and a page size of 16K bytes and 512MB of physical memory. If each entry in the page table is 6 bytes, what is the maximum size of the page table?

$32 - (\log_2 16K) = 32 - 14 = 18$

$2^{18} \cdot 6 \text{ bytes} = 1,572,860$

Page Table size = 1,572,860 (in bytes)

2. *(5%)* Under what conditions would two levels of cache make sense?

IF making the First cache larger slows it down an extra clock, it may make sense to have a smaller First level cache and a larger second level cache.

3. *(5%)* What is the average time to read or write a sector on a 15,000RPM disk drive with an average seek time of 8ms, a transfer rate of 10.0 MB/sec, and 1024-byte sectors. Assume the disk is idle and there is a 0.25 ms controller overhead per sector.

$8\text{ms} + \frac{0.5\text{RPM}}{1500\text{RPM}/60\text{RPM/sec}} + \frac{1024\text{ bytes}}{10\text{MB/sec}} + .25\text{MS} =$

$8 + 2 + .1 + .25 = 10.35\text{ms}$

Average R/W time per sector = 10.35 (in ms)

4. *(5%)* Which type of bus (synchronous or asynchronous) would work best in a system where the bus length and loading did not vary? (explain).

synchronous - since loading and length are fixed it would be faster

5. *(5%)* The new USB 2.0 standard is a 1-bit serial bus with a 480Mhz clock. What is that bandwidth in megabytes per second?

$480\text{MHz} / 8\text{bits/byte}$

Bandwidth = 60 (in Mbytes/second)

6. *(5%)* Would a long CPU bound job be inserted more often in the ready queue or the wait queue (explain)?

ready queue - Since it uses many CPU clocks, it will be interrupted and inserted into the ready queue waiting for CPU. wait queue is for I/O waits.

7. *(5%)* Why should the scheduler attempt to control the degree of multiprogramming?

more processes can improve CPU utilization since when some are waiting others can run. Too many processes might compete for resources such as memory and slow down

8. *(5%)* Other than memory, a processor with a cache, and a disk drive with DMA, what other two important hardware features would be critical to support a modern multi-user Unix-like operating system? (Explain)

Virtual Memory - cache disk and add memory protection
Timer to generate interrupts - used for time slice interrupts

9. *(5%)* What conditions must be present for the possibility of a deadlock (Without considering the inner details of process's code)?

multiple processes running
processes can hold a resource while waiting on another resource

10. *(5%)* Using the Text's notation, add a semaphore called A to the processes below so that they will function correctly with the shared variable V. V is the only shared variable and all references to V are shown. Semaphore A does not need to be declared in each process.

perhaps optional if one instruction needed.

P0	**P1**	**P2**
.	.	P(A)
.	.	**V=0;**
.	.	V(A)
P(A)	P(A)	.
IF V=W Then V=X;	**If V=Z then V=Y;**	.
V(A)	V(A)	.

Set Associative Cache Memory

11. (*15%*)A two-way set associative cache is given the memory operations shown below. It contains four lines and has one word per block. A LRU (Least Recently Used) replacement policy is used on this cache. The cache is initially empty. The first column of the cache gets the first entry after the valid bits have been reset. In the blanks provided in the Cache below, list the original address value only (i.e. 12 in blank, means address and data for memory location 12 is in cache).

Memory Read Operations

Address	Hit (Y/N)?
0	N
1	N
2	N
3	N
4	N
20	N
21	N
5	N
6	N
3	Y
4	Y
20	Y
21	Y
5	Y
6	Y
3	Y

Cache Contents

Block	Element 1	Element 2
0	~~0~~ 20	4
1	~~x~~ 5	21
2	2	6
3	3	

Hit rate for all memory operations is 43.75 (%)

Virtual Memory

12. *(15%)* Assume a 16-entry direct-mapped TLB is used in a system with 28-bit virtual byte addresses, 20-bit physical byte addresses, and 256 byte pages. For the sequence of virtual addresses shown below, state whether each address causes a TLB hit or miss and show the physical address generated. Portions of the initial contents of the TLB and full page table are given. Assume all listed page table entries are valid. Show the final contents of the TLB after this sequence of addresses is accessed.

Virtual address sequence

Address	*Hit/Miss*	*Physical Address*
0000013	H	200 13
00022CF	H	A00 CF
00023A1	M	E20 A1
0000101	M	F00 01
00000FF	H	200 FF
0002015	M	7 1 0 1 5
0002266	H	A00 66

TLB Initial Contents

Block	*Tag*	*Data*
0	~~0000~~ 0002	~~200~~ 710
1	~~0002~~ 0000	~~C00~~ F00
2	0002	A00
3	~~0020~~ 0002	~~E20~~ E20

TLB Final Contents

Block	*Tag*	*Data*
0	0002	710
1	0000	F00
2	0002	A00
3	0002	E20

Page Table Initial Contents

Virtual Page #	*Data*
00000	200
00001	F00
00002	550
00003	300
…	
00020	710
00021	C00
00022	A00
00023	E20

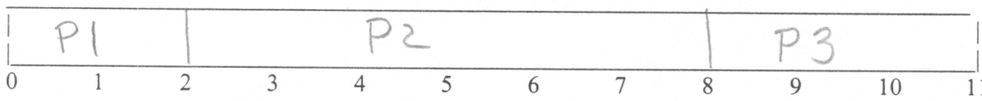
CPU Scheduling

13. (20%) The following processes arrive for execution at the times indicated. Use preemptive scheduling for SRTF and RR and base all decisions on the information you have at the time the decision is made. At arrival time, the burst execution time is known. **Note:** For RR assume a process is already added to the end of the ready queue by the arrival time when the scheduler checks the queue and the ready queue will execute in strict FIFO order at each time slice(i.e. if a process is already in the ready queue before another arrives, it will execute first).

Process	Arrival Time	CPU Burst or Execution Time
P1	0.0ms	2ms
P2	1.0ms	6ms
P3	2.0ms	3ms

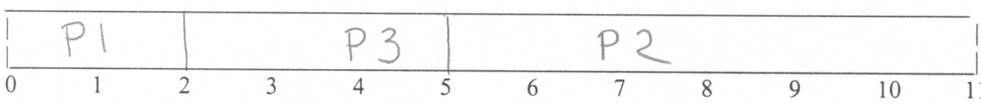
Draw a Gantt chart using FCFS:

T.T. $\frac{2+(8-1)+(11-2)}{3}$



W.T. $\frac{0+1+(8-2)}{3}$

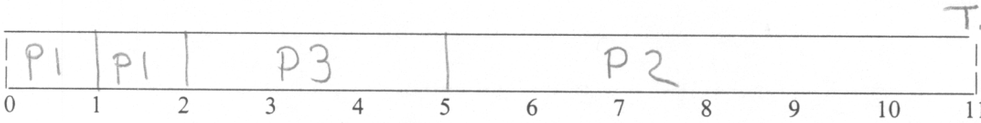
Draw a Gantt chart using SJF (no preemption):



Same

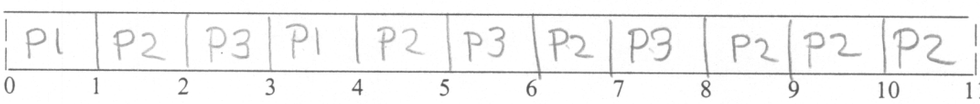
Draw a Gantt chart using SRTF:

T.T. $\frac{2+3+10}{3}$



Draw a Gantt chart using RR with time slice =1:

W.T. $\frac{0+0+(5-1)}{3}$



Fill in the table below:

T.T. $\frac{4+(11-1)+(8-2)}{3}$

	Average Turnaround Time	Average Wait Time
FCFS	6	2.333
SJF	5	1.333
SRTF	5	1.333
RR	6.667	3

W.T. $\frac{2+4+3}{3}$